Energy Monitoring System for Security and Energy Management Applications

by

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ABSTRACT

ENERGY MONITORING SYSTEM FOR SECURITY AND ENERGY MANAGEMENT APPLICATIONS

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This thesis presents an energy monitoring system to measure energy consumption of software applications to support security and power management for embedded devices. The proposed system is composed of an Actel Fusion device and a custom designed energy measurement circuit. The Fusion device measures the voltage and the current of the target device at a defined sampling rate. The energy measurement circuit is designed as a current integrator over fixed intervals using the switched-capacitor integrator technique to store energy information of the target device within Fusion’s sampling intervals. This circuit is designed to accommodate the low sampling rate of the Fusion device.

Experimental results showed that the Fusion device allows the measurement of the energy of the target device at a minimum rate of 15 µs. The energy measurement circuit is implemented using the 65 nm CMOS technology. Simulation results showed that this circuit provides 91%~97% average energy measurement accuracy.
I owe my biggest thanks to my advisor, Dr. Radu Muresan. Without his help this project would not have been possible and without his support I would not stand where I am today. I would also like to thank my co-advisor, Dr. Anthony Vannelli, for funding this project. Thanks to the School of Engineering system information specialist, Joel Best, for technical support.

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My deepest thanks to my family. Thanks to my sisters, Azadeh and Mahnaz, who encouraged me to continue my education. Most of all, thanks to my parents, Hamid and Azar, for their unconditional love and support.
# Contents

Acknowledgement .......................................................................................................................... iii
List of Tables ................................................................................................................................. vi
List of Figures ............................................................................................................................... vii
Chapter 1: Introduction .................................................................................................................. 1
Chapter 2: Literature Review ......................................................................................................... 5
  2.1 Security Management Systems ............................................................................................... 5
  2.2 Battery and Energy Management Systems ............................................................................ 6
  2.3 Energy Monitoring Systems .................................................................................................. 9
  2.4 Summary ................................................................................................................................ 12
Chapter 3: Background .................................................................................................................. 13
  3.1 Overview of Actel Fusion Mixed-Signal FPGA Platform ....................................................... 13
    3.1.1 Integrated Analog Interface ............................................................................................ 15
    3.1.2 Programmable Timer ..................................................................................................... 19
  3.2 Switched-Capacitor (SC) Integrator Circuit ........................................................................... 19
    3.2.1 Theory of Operation ....................................................................................................... 21
  3.3 Summary ................................................................................................................................ 23
Chapter 4: Proposed Design .......................................................................................................... 24
  4.1 Design Goal ............................................................................................................................ 24
  4.2 Methodology ......................................................................................................................... 24
  4.3 IP Core Architecture of the Actel Fusion Mixed-Signal FPGA Device ................................. 26
    4.3.1 Actel Fusion Hardware Design ....................................................................................... 27
    4.3.2 Actel Fusion Software Design ....................................................................................... 30
List of Tables

Table 3.1: Fusion common IP cores ............................................................................................................. 14
Table 4.1: Design specifications ................................................................................................................ 43
Table 5.1: Execution time for Fusion device ............................................................................................ 48
Table 5.2: Differential amplifier simulated results .................................................................................. 53
Table 5.3: Integration results at each rest points ...................................................................................... 59
Table 5.4: Energy conversion constants (K and A) for each input waveform ........................................ 61
Table 5.5: Average error values for sine, pulse, ramp and irregular input waveforms ...................... 64
Table 5.6: Energy conversion constants (K and A) for irregular input waveforms .............................. 69
Table 5.7: Average error values for irregular input waveforms. .............................................................. 69
List of Figures

Figure 3.1: Analog interface architecture of the Fusion device .......................................................... 15
Figure 3.2: Monitor block of the analog quad structure ................................................................. 16
Figure 3.3: A non-inverting switched-capacitor integrator circuit ...................................................... 20
Figure 3.4: A pair of non-overlapping clock signals (CLK1 and CLK2). ............................................. 21
Figure 3.5: Switched-capacitor integrator circuit during clock phases: (a) CLK1, (b) CLK2 ............. 22
Figure 4.1: Schematic of the energy monitoring system composed of the Actel Fusion mixed-signal FPGA device and the energy measurement circuit. .............................................................. 25
Figure 4.2: Actel Fusion mixed-signal FPGA device on-chip IP cores architecture used for generating the hardware-based interrupt system and performing required measurements .......... 28
Figure 4.3: Implemented hardware platform of IP cores connection on the SmartDesign canvas. .................................................................................................................................................. 31
Figure 4.4: Basic diagram for the measurement cycle program ........................................................... 32
Figure 4.5: Energy measurement circuit (a detailed schematic is shown in Appendix) ......................... 35
Figure 4.6: Non-overlapping clock generation schematic (the transistor level schematic is shown in Appendix). ........................................................................................................................................... 38
Figure 4.7: CMOS differential amplifier using a p-channel current-mirror load (the detailed schematic is shown in Appendix) ........................................................................................................... 40
Figure 5.1: The experimental setup for Fusion device ............................................................................ 45
Figure 5.2: Sampled voltage for three periods of the inputted square waveform ................................... 47
Figure 5.3: Voltage transfer curve for the differential amplifier of Fig. 4.7 ........................................... 50
Figure 5.4: Maximum output voltage of the differential amplifier of Fig. 4.7 ...................................... 51
Figure 5.5: Simulated dc gain, unity-gain frequency and phase margin of differential amplifier of Fig. 4.7 ................................................................. 52

Figure 5.6: Input sine waveform and its integration output results. ............................................. 54

Figure 5.7: Input pulse waveform and its integration output results. ......................................... 55

Figure 5.8: Input sawtooth waveform and its integration output results. ................................. 56

Figure 5.9: Input ramp waveform and its integration output results ........................................ 57

Figure 5.10: Input irregular waveform and its integration output results .................................. 58

Figure 5.11: Input irregular1 waveform and its integration output results ................................ 62

Figure 5.12: Input irregular2 waveform and its integration output results ................................ 62

Figure 5.13: Input irregular3 waveform and its integration output results ................................ 63

Figure 5.14: Comparison of sine waveform circuit and calculator output results ...................... 65

Figure 5.15: Comparison of pulse waveform circuit and calculator output results ...................... 65

Figure 5.16: Comparison of sawtooth waveform circuit and calculator output results ............... 66

Figure 5.17: Comparison of ramp waveform circuit and calculator output results ..................... 66

Figure 5.18: Comparison of irregular waveform circuit and calculator output results ............... 67

Figure 5.19: Comparison of irregular1 waveform circuit and calculator output results ............. 67

Figure 5.20: Comparison of irregular2 waveform circuit and calculator output results ............. 68

Figure 5.21: Comparison of irregular3 waveform circuit and calculator output results ............. 68

Figure A.1: Energy measurement circuit ................................................................. 80

Figure A.2: Non-overlapping clock generation schematic ...................................................... 81

Figure A.3: CMOS differential amplifier using a p-channel current-mirror load ....................... 82
Chapter 1: Introduction

With the increased use of embedded systems in secure applications, such as banking, healthcare and transportation, and portable devices, such as cellular phones, personal digital assistants (PDAs) and notebook computers, security and energy\(^1\) management in embedded systems have become more essential. Security management is required in order to protect personal information and provide secure communications, while energy management intends to save energy in general and to increase battery lifetime of portable devices in particular.

In secure applications, the secret key of cryptographic devices (e.g., smart cards, e-passport, etc.) is embedded; however, it can be attacked by extracting some side-channel information of the device such as the instantaneous power consumption of the device. Therefore, in embedded devices, power consumption influences the security of the device. These attacks based on power consumption information are known as power analysis attacks (PAA) [1]. There exist various countermeasures against PAA at the hardware and software levels. One of the countermeasures against PAA is the current flattening technique implemented at the software level [2]. However, implementing effective current flattening at the software level relies on energy consumption information at the instruction level [2]. In order to obtain the energy consumption information, an accurate energy monitoring system is required.

In portable devices, in order to optimize their battery lifetime, a number of dynamic power

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\(1\) In this work, we will use the term energy and power interchangeably since one can be easily obtained from the other one.
management (DPM) techniques have been proven to be effective. The most well known DPM techniques are battery cell scheduling charge and discharge algorithms [3], [4], [5], [6] and dynamic voltage scaling (DVS) [7], [8]. Critical to the effective application of these techniques is the ability to monitor and profile the power consumed by the device.

Energy and power consumption information can be obtained by a number of approaches. The most common approaches can be categorized as either measurement-based or estimation-based approaches. A measurement-based approach is based on physical energy and power measurement [9], [2] whereas an estimation-based approach is based on power models [10], [11], [12], [13]. A special form of the estimation-based approach is called power emulation. Power emulation obtains power consumption information from a power measurement circuit and maps this information into a hardware prototyping platform such as field-programmable gate array (FPGA) boards [14], [15], [16]. Due to the programmability and accuracy of FPGAs, this approach is of increased interest.

The goal of this thesis is to present a real-time system-on-chip (SoC) energy monitoring system for security application and energy management for embedded devices. The energy monitoring system we proposed comprises a mixed-signal FPGA device accompanied with a complementary metal oxide semiconductor (CMOS)-based energy measurement circuit. Of all mixed-signal FPGA devices, Fusion from Actel Corporation, as the first high performance mixed-signal FPGA device, offers various advantageous features [17]. The Fusion device integrates a number of intellectual properties (IP) cores that can be used to configure various SoC architectures and, in addition, Fusion contains programmable logic for both analog and digital applications. The key feature of the Fusion device is its capability of monitoring voltage, current and temperature of any device. Thus, this feature provides stand-alone energy measurement.
In this work, we made use of the Fusion’s programmability to sample the voltage and the current of any embedded application at a fixed sampling rate in order to determine the energy consumption of the device. However, since the maximum frequency of the analog interface (AI) of the Fusion device is limited [18], this affects the sampling rate of the Fusion device. Therefore, there is a need for an IP core to accumulate the energy information of the target device between the Fusion’s sampling intervals in order to compensate for Fusion’s low sampling rate. For this reason, we developed an energy measurement circuit that is capable of integrating the current of the target device over time. Since the voltage variation in each sampling interval is considerably small, voltage can be assumed constant within Fusion’s sampling intervals and therefore, the profile of the current obtained from the energy measurement circuit is sufficient to determine the energy consumed by the device. The energy measurement circuit is proposed as a custom chip using switched-capacitor (SC) integrator technique which is designed, implemented and tested in the 65 nm CMOS technology. Initial simulation results of an energy measurement circuit implemented in 0.18 μm CMOS technology have been reported in [19].

The main achievements of this thesis are summarized as follows:

- Development of hardware IP cores architecture for the Actel Fusion mixed-signal FPGA device as well as its software program application in order to support all targeted interfaces.
- Implementation of a CMOS-based energy measurement circuit in 65 nm technology to accumulate the instantaneous current of the target device over time.
• Formulation of the relationship between energy measurement circuit results and mathematical integration results (ideal results) to derive associated energy conversion constants.

• Evaluation of the accuracy of the derived energy conversion constants through various simulation experiments and calculation of the average error.

This thesis is organized as follows: Chapter 2 is a literature review of previous works on security, battery and energy management systems as well as a presentation of various approaches to monitor energy and power of the embedded devices. Chapter 3 presents the brief background on functionality and features of Actel Fusion mixed-signal FPGA device, the description of the various components of SC integrator circuits and the basic working principle of SC integrator operation. Chapter 4 presents our methodology, the hardware and software design of the Actel Fusion mixed-signal FPGA device, the components of our proposed energy measurement circuit in details, the analysis of the design and the design constraints. Chapter 5 presents the experimental results of the Fusion device and the simulation results of the energy measurement circuit to verify the functionality of our energy monitoring system. Finally, Chapter 6 concludes the thesis and discusses possible future work.
Chapter 2: Literature Review

As previously mentioned, the energy consumed by the embedded device impacts the security of the system and the battery lifetime. In this chapter, we review some of the previous research on security, battery and energy management systems in order to understand the motivation for energy monitoring system. Furthermore, we discuss some related works on various approaches to energy and power monitoring systems.

2.1 Security Management Systems

There exist different types of attacks that can be an extensive threat to the security of an embedded device. One of the most effective types of attacks is power analysis attacks (PAA). PAA are based on power consumption information leaked during encryption or decryption operations [1]. Since the power consumption of the embedded devices depends on performed operations and processed data, in PAA the attacker estimates the power dissipation and guesses the secret key based on an analysis of power traces.

PAA is a passive and non-invasive technique. The former indicates that the attacker reveals the secret key by observing the physical property of the device (power consumption in PAA case) and the latter implies that no evidence of attack can be observed from the device since the attack does not modify the device permanently. There are two main categories of attacks based on power consumption analysis: simple power analysis (SPA) attacks and differential power analysis (DPA) attacks. SPA use few power traces to reveal the dependency of performed cryptographic operations (e.g., multiplication, branches, squaring and shifts) on power consumption in a direct manner (i.e., visual observation) whereas DPA, first introduced in [20], is more
complex and uses a large number of traces combined with statistical analysis to retrieve the secret key of encryption algorithms such as data encryption standard (DES), advanced encryption standard (AES) and etc.

Various countermeasures against PAA at software and hardware levels have been introduced in literature [1]. Of these, current flattening technique at software level is related to this research [2]. The purpose of the current flattening technique is to reduce the dependency of the performed operations and processed data to variations of current consumption at the attacker observation point.

In [2], Muresan and Gebotys introduced the current flattening technique implemented at the software level by inserting non-functional instructions (NFIs) within the program which do not consume additional registers and do not modify the functionality of the program. The goal of NFIs insertion is to maintain the current consumption profile of the code fairly constant (within the defined current variation limits). In this way, the dependency of the variation of the current consumption on the processed data is reduced at the attacker observation point (i.e., the power supply pin). Their simulation results showed 78% reduction in data and current consumption dependencies. The major challenge of this technique is to perform decision making on the number of NFIs required and the locations in which they are to be inserted.

2.2 Battery and Energy Management Systems

The use of portable devices is certainly dependent on their batteries. Considering the batteries as a limited source of energy with high cost makes energy management for batteries a primary design factor. Energy management reduces the cost of design due to the corresponding
cooling cost and assures longer battery lifetime. Battery lifetime refers to the number of charge and discharge cycles the battery may perform before it becomes unusable [21].

Energy management techniques can be categorized as static techniques and dynamic techniques as the power consumption of the device is the sum of static and dynamic power consumption. Static power consumption is the baseline power consumed by the device, even while the device is not operating, whereas the dynamic power consumption is mainly due to the switching activity of the device [22]. Static techniques are beyond the scope of this research; in this subsection, therefore, we only review some dynamic techniques.

Dynamic techniques are known as dynamic power management (DPM). Several DPM techniques have been proposed to provide efficient energy management in embedded devices. A common technique to DPM is battery cell scheduling charge and discharge algorithms. A simplest example of battery cell scheduling algorithm is a sequential discharge algorithm [3] where battery cells discharge by switching from one cell to the next cell while the amount of charge of the first cell is lower than the threshold. A more effective algorithm was proposed in [4], where the researchers developed the parallel battery cell discharge algorithm for multi-battery systems which controls the battery discharge rate by switching between two or more battery cells based on the load current profile. Their results showed a significant improvement (160%) in comparison to sequential discharge algorithms. In [5], the authors proposed a reconfigurable battery pack containing a management unit in order to schedule cells to be discharged based on the load current. Their simulation results found improvement in battery lifetime of approximately 22%. Another algorithm for battery scheduling was proposed in [6]. Their so-called weighted k-round-robin (kRR) algorithm discharges k-cells in parallel, where k is estimated by instantaneous
energy consumption of the load. Their results showed 56% longer battery lifetime in comparison to sequential algorithms.

An additional technique to DPM is dynamic voltage scaling (DVS). This technique adjusts the supply voltage dynamically to multiple levels based on energy demand of the workload. Dynamic power consumption can be given by:

\[ P_{\text{Dynamic}} = C \cdot V^2 \cdot F \]  \hspace{1cm} (3.1)

where \( C \) is the switching capacitance, \( V \) is the supply voltage and \( F \) is the operating frequency. Given this relationship, the variation in supply voltage is directly proportional to dynamic power variations [23]. For this reason, supply voltage adjustment is a promising technique for dynamic power reduction. In [7], Visairo and Kumar proposed to reconfigure the cells’ internal connections from series to parallel or vice-versa based on load current profile in order to scale the input voltage. With their reconfigurable battery pack, they obtained a battery lifetime extension of 15 minutes. In [8], Bondade and Ma implemented an embedded power management module composed of single-inductor multiple-output (SIMO) and on-line power sensor. The SIMO provided a wide range of variable supply voltage (i.e., from 0.9 V to 3 V) based on the instantaneous power consumption sensed by the power sensor.

While such techniques successfully extended the battery lifetime, the development of these techniques demands an efficient methodology for an energy monitoring system to profile the energy or current drawn from the device during execution of the program applications.
2.3 Energy Monitoring Systems

Several approaches have been studied in order to obtain energy and power information. These approaches are categorized as measurement-based and estimation-based.

The measurement-based approach collects energy and power information by actual physical measurement [9], [2]. In [9], Flinn and Satyanarayanan developed the PowerScope tool for sampling the energy consumption of a mobile system at a defined period. PowerScope sampled the current drawn from the device by means of a Hewlett Packard 3458A digital multimeter. The sampling period was approximately 1.6 ms. The output of multimeter (current information) was collected and analyzed on a separate host computer. In [2], Muresan and Gebotys proposed a real-time power analysis attack resistant architecture, called PAAR, for on-chip analog power measurement and current flattening purposes. The architecture is composed of resistor-based current sensors, differential amplifier, digital to analog convertor (D/A) and comparators to control the power consumption of the system dynamically. This current flattening measurement can be further combined with principles such as voltage scaling and frequency scaling for energy and power management purposes [24]. Although power monitoring by means of a measurement-based approach is very accurate, it increases the size of the design.

Estimation-based approach is based on power modeling which is less accurate in comparison to the measurement-based approach, and is not suitable for complex applications. However, estimation-based approach reduces the size of the design. Estimation-based approach can be further categorized as simulation-based and hardware-accelerated approaches.

The simulation-based approach [10], [11] achieves energy and power information by executing power model programs on simulators. However, since the power characteristics of each
component of the system (e.g., processors, memories and custom IP blocks) differ from the others, deriving a single model to cover the power characteristics of all components is extremely difficult. For this reason in [10] Lee and et al. proposed to employ different power models for various components of the system. They developed a simulation framework that contained a processor core model (modeled for two basic states: busy and idle), a cache model (modeled as an accumulation of power values for all accessed SRAM modules), a bus model (modeled based on different components such as decoders and routers) and a memory model (modeled by power per read, write and idle operations). Their power models provided power consumption information concurrently and showed more than 90% power estimation accuracy. Another simulation-based power model was proposed in [11] where the researchers developed an instruction set simulator. The simulator calculates the total energy dissipation of the system composed of instruction energy dissipation, data energy dissipation, cache system energy dissipation and external components energy dissipation (e.g., bus system, memories and peripherals).

However, the simulation-based approach is commonly used for non-real-time estimation as simulators require extensive simulation time. Therefore, to address real-time estimation, the hardware-accelerated approach was introduced.

In the hardware-accelerated approach [12], [13] energy and power information is obtained from a power model implemented in a dedicated hardware circuit. An example of the hardware-accelerated approach is to use existing hardware performance counters (HPCs) of processors to track power events that can be used to estimate the processor power consumption [12]. However, using these counters increases the power estimation time and, in this system, limits the power estimation to offline analysis. To overcome these issues, in [13], Peddersen and Parameswaran suggested adding 32-bit increment counters to processor’s original hardware. These counters al-
low power consumption estimation by detecting and counting the system’s power consumption events during run-time. However, implementing these counters may not be possible for general embedded processors.

A special type of hardware-accelerated approach is a power emulation approach, initially introduced in [14]. A power emulation approach is typically performed by an energy and power measurement circuit incorporated into a FPGA prototyping platform. In [14], the authors developed the power model enhanced circuit composed of power models, to monitor and compute power values for individual input signals, and a power aggregator, to calculate the total power consumption. The power model enhanced circuit targeted the Xilinx Virtex-II FPGA. By performing a power emulation approach they achieved significant run-time reduction (10x to 500x compared to commercial power estimation tool). Another Xilinx Virtex-II FPGA-based power monitoring system was proposed in [15]. This system used the FPGA device in conjunction with event counters to estimate power consumption of running applications. Their results indicated that this system has within 10% average error in comparison to software simulators. More recently, in [16], the emulation-based real-time power monitoring architecture was proposed. This architecture integrated a number of power sensors to track power information of system and its subcomponents. The power information was stored in a software-configurable table and it was transmitted to a power estimation hardware unit to be accumulated. This power emulation architecture was compared to the power simulation-based approach and the relative error was reported to be below 10%. They further showed this power profiling method can be used to detect critical regions that lead to power peaks during execution of embedded software application. They illustrate the effectiveness of their approach on a deep-submicron smart card microcontroller sys-
tem [25]. While power emulation approach decreases the run-time, it increases the size of the design.

Some of the studies presented here provided energy and power information by means of on-chip energy measurement circuits. Others applied power simulators or FPGA-based power emulators. Our intention is to design an energy monitoring system to provide the information of the energy consumption for high-level software applications. Our system is based on an Actel Fusion mixed-signal FPGA device along with an on-chip energy measurement circuit using SC integrator technique. The concept of an energy monitoring system composed of the Fusion FPGA board and a SC integrator circuit was initially explored in [19], where the authors used a SC integrator circuit to accumulate energy over time to compensate for Fusion’s low sampling rate. They implemented their SC integrator circuit in 0.18 μm CMOS technology and showed their experimental results. However, in this thesis, we implement the complete hardware IP core architecture of the Fusion device as well as its software application program, we propose energy measurement circuit based on SC integrator technique in nonoscale (65 nm) technology and we investigate the relationship between our energy measurement circuit’s results and mathematical model results (i.e., ideal results) in order to derive associated energy conversion constants.

2.4 Summary

This chapter presented a literature review of security, battery and energy management systems and showed that designing an energy monitoring system for these systems is increased of interest. Also, this chapter presented the various approaches to monitor energy and power consumption information. These approaches can be implemented by means of physical measurement or power models. More recently, power measurement by means of FPGA prototyping platform has gained much attention.
Chapter 3: Background

In order to gain a better understanding of the components of our proposed energy monitoring system, this chapter presents an overview of the functionality and features of the Actel Fusion mixed-signal FPGA device, and also the analysis of the switched-capacitor (SC) integrator technique as a part of our proposed energy measurement circuit.

3.1 Overview of Actel Fusion Mixed-Signal FPGA Platform

Fusion from Actel Company is the first mixed-signal FPGA device that offers advantageous features for a variety of applications, especially for power management and clock generation. The key features of Fusion is its low power characteristics, its programmable analog interface that supports a variety of mixed-signal applications and also its on-chip clock resources such as an analog phase-locked loop (PLL) and a high frequency RC oscillator.

The Fusion device integrates an embedded processor Cortex-M1 from ARM family and a number of intellectual property (IP) cores in a single monolithic programmable chip [18]. Thus, it simplifies the design and results in system cost savings and space reduction. Cortex-M1 is a 32-bit configurable processor designed and optimized specifically for FPGAs implementation [26]. The combination of the Cortex-M1 processor and IP cores can be used to configure various SoC architectures. The most common Fusion IP cores, their categories and the description of their functionalities are summarized in Table 2.1.
<table>
<thead>
<tr>
<th>IP Core</th>
<th>Category</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CoreAhhNVM</td>
<td>Memory and Controllers</td>
<td>Allows access to the 1 MByte internal embedded flash non-volatile memory (NVM).</td>
</tr>
<tr>
<td>CoreAhhSRAM</td>
<td>Memory and Controllers</td>
<td>Provides interface for writing and reading the 30 Kbytes internal static random access memory (SRAM).</td>
</tr>
<tr>
<td>CoreMemctrl</td>
<td>Memory and Controllers</td>
<td>Controls reading and writing operations between the flash memory and SRAM.</td>
</tr>
<tr>
<td>CoreAI</td>
<td>Peripherals</td>
<td>Allows configuring, controlling and interacting with analog interface.</td>
</tr>
<tr>
<td>CoreTimer</td>
<td>Peripherals</td>
<td>Operates as an interrupt-generating programmable decrementing counter to interrupt Cortex-M1 over fixed or variable sampling intervals.</td>
</tr>
<tr>
<td>CoreGPIO</td>
<td>Peripherals</td>
<td>Allows access to general purpose input/output (GPIO). This core provides access up to 32 inputs and 32 outputs.</td>
</tr>
<tr>
<td>CoreUART</td>
<td>Peripherals</td>
<td>Provides connection to an off-chip universal serial bus (USB)-to-universal asynchronous receiver/transmitter (UART) and allows transmitting and receiving operations.</td>
</tr>
<tr>
<td>CoreAHBLite</td>
<td>Bus Interfaces</td>
<td>A 32-bit advanced high-performance bus (AHB) interface that can be connected up to 2 masters and 16 slave peripherals.</td>
</tr>
<tr>
<td>CoreAPB</td>
<td>Bus Interfaces</td>
<td>A 32-bit advanced peripheral bus that can be connected up to 16 peripherals. Typically, CoreAPB interfaces low-speed IP core devices.</td>
</tr>
<tr>
<td>CoreAHB2APB</td>
<td>Bus Interfaces</td>
<td>A bridge to connect AHB bus to APB bus.</td>
</tr>
</tbody>
</table>
Of these IP cores, the analog interface (CoreAI) and the timer (CoreTimer) are our primary interests since our goal is to make use of Fusion’s configurable analog components and programmable interrupt-generating timer to perform voltage and current measurements at fixed intervals. The functionality of these IP cores is discussed in details in the following subsections.

### 3.1.1 Integrated Analog Interface

One of the key features of the Fusion device is its configurable analog interface. The overview of the analog interface architecture is shown in Fig. 3.1. It contains 10 analog quads, a 32:1 input analog multiplexer and a configurable analog-to-digital converter (ADC).

![Analog interface architecture of the Fusion device](image)

**Figure 3.1: Analog interface architecture of the Fusion device**

The analog quad preconditions the analog signals prior to conversion to digital signals [18]. The analog quad comprises three monitor blocks: voltage, current and temperature monitor blocks. For energy management purposes, only the first two monitor blocks (i.e., voltage and
current) are in use. Fig. 3.2 illustrates the simplified schematic of the voltage (or current) monitor block of the analog quad structure.

![Diagram of Monitor block](image)

**Figure 3.2: Monitor block of the analog quad structure**

In the voltage monitor block, the $A_V$ pad is used to monitor the voltage source. As shown in Fig 2.2, this monitor block consists of a prescaler circuit and a 2:1 multiplexer. The prescaler circuit includes programmed scaling factors to ensure that the analog input signal is in a proper input range of the Fusion device (from 0 to voltage reference). The 2:1 multiplexer conveys the scaled signal to the 32:1 analog multiplexer to be sent to the ADC.

In current monitor block, the $A_C$ pad is used to perform current measurement of the target device. The functionality of the current monitor block is similar to the voltage monitor block with only one difference, which is the presence of an external sense resistor connected to the $A_C$ pin. The current measurement is obtained by calculating the voltage drop across this resistor. Thereafter, this voltage drop passes a Fusion built-in differential amplifier with the amplification...
factor of 10. This amplifier is used to increase the accuracy of the current measurement and also to reduce the resistance of the external sense resistor. To obtain the current of the target device, the following relation must hold:

$$|I| = \frac{ADC \cdot V_{ref}}{R_{Actel \cdot 10 \cdot 2^N}}$$  \hspace{1cm} (3.1)

where, $ADC$ is the result obtained from conversion, $V_{ref}$ is the reference voltage of the Fusion device, $N$ is the ADC’s operation mode and $R_{Actel}$ is the resistance of the external sense resistor. Since there exists 10 analog quads, up to 30 analog input signals can be converted to their equivalent digital values.

The 32:1 analog multiplexer is the input to the ADC (See Fig. 3.1). The 30 input channels of this multiplexer are defined by analog quads and the two remaining input channels are dedicated to monitor power supply and device temperature [18]. The analog multiplexer contains a five-pin interface (CHNUMBER [4:0]) in order to determine which channel is selected to be sent to the ADC.

The ADC can operate in 8-, 10- or 12-bits mode. The period of the ADC’s internal clock ($T_{ADC,CLK}$) is determined by the system clock period ($T_{SYS,CLK}$) and a time divider control ($TVC$) programmable input signal, and it is equal to:

$$T_{ADC,CLK} = 4 + (1 + TVC) \cdot T_{SYS,CLK}$$  \hspace{1cm} (3.2)

The Fusion’s ADC conversion cycle is accomplished in three phases: sampling, distribution and post-calibration [18]. In the sampling phase, the ADC samples the analog input signal. The
The time of sampling ($T_{\text{sample}}$) is controlled by the ADC’s internal clock period ($T_{\text{ADC,CLK}}$) and a sample time control ($STC$) programmable input signal, as expressed in:

$$T_{\text{sample}} = (2 + STC) \cdot T_{\text{ADC,CLK}} \quad (3.3)$$

In distribution phase, the ADC converts the analog input signal to its digital corresponding value. The distribution time ($T_{\text{distrib}}$) is dependent on the ADC’s internal clock period ($T_{\text{ADC,CLK}}$) and the ADC mode ($N$):

$$T_{\text{distrib}} = N \cdot T_{\text{ADC,CLK}} \quad (3.4)$$

In post-calibration phase, the ADC conversion cycle is complete and digital values are ready to be read. This phase is not mandatory, however, it is recommended for conversion accuracy. The post-calibration time ($T_{\text{post,cal}}$) is given by:

$$T_{\text{post,cal}} = 2 \cdot T_{\text{ADC,CLK}} \quad (3.5)$$

As a result, the whole conversion time ($T_{\text{conv}}$) includes the time allocated to these three phases in addition to the time for the ADC to perform reading and writing operations. Therefore, the conversion time can be derived as [18]:

$$T_{\text{conv}} = T_{\text{sample}} + T_{\text{distrib}} + T_{\text{post,cal}} + T_{\text{read}} + T_{\text{write}} \quad (3.6)$$

The above relationships imply that Fusion’s ADC’s internal clock frequency ($\frac{1}{T_{\text{ADC,CLK}}}$) is an important factor in Fusion’s conversion time. This frequency is limited up to 10 MHz [18]. Therefore, the most important challenge involved in system design by means of the Fusion device is compensation for the low frequency of the Fusion’s analog interface.
### 3.1.2 Programmable Timer

For our implementation, the programmable timer operates as an interrupt-generating decrementing counter. It uses defined load value, programmable modes and prescaler unit to create the interrupt at a defined period.

The process operation of this IP core is as follows: initialization of the timer sets the load value to the decrementing counter and causes the counter to start decreasing. The load value is the value from which the timer’s counter will decrease. When the decrementing counter reaches zero the interrupt is generated.

The timer can operate in two modes: continuous mode and one-shot timer mode. The default mode is the continuous mode which automatically reloads the load value to the decrementing counter on reaching zero. Therefore, the continuous mode is suitable for the system with the periodic interrupt. While in one-shot timer mode, the system halts on reaching zero and the decrementing counter should be programmed to start the new decreasing cycle.

The prescaler unit is used to divide down the system clock frequency by a factor of 2, 4, 8, 16, 32, 64, 128, 256, 512 or 1024 in order to allow the decrementing counter to function using a lower frequency than the system clock frequency [27]. More details about Fusion IP cores are reported in Actel Fusion datasheet [18].

### 3.2 Switched-Capacitor (SC) Integrator Circuit

A switched-capacitor (SC) integrator circuit is one of the common electrical networks in analog and mixed-signal integrated circuit design. Some typical SC integrator circuit applications include ADCs and filters [28]. The SC integrator provides an accurate integration by switching a
sampling capacitor \( (C_1) \) into an amplifier with a feedback integration capacitor \( (C_2) \). Fig. 3.3 illustrates a non-inverting SC integrator circuit [29], [30].

![SC integrator circuit diagram](image)

**Figure 3.3: A non-inverting switched-capacitor integrator circuit**

As shown in Fig. 2.3, the SC integrator circuit consists of switches, non-overlapping clocks, capacitors and a differential amplifier. The switches control the charge flow of the circuit while they are ON and OFF. MOS transistors are suitable for switches as they provide high resistance (in gigaoohms range) while they are OFF and they have low resistance while they are ON (several kilohms [31]). Therefore, MOS transistors as switches reduce the charge leakage and allow fast charging [28]. In addition, the MOS transistors have higher integration density in comparison to their bipolar equivalent [32].

The switches are turned on and off by a pair of non-overlapping clocks. The purpose of the non-overlapping clocks is to determine the charge transfer operation. The non-overlap time ensures that the switches are not ON simultaneously. The non-overlapping clock signals are shown in Fig. 3.4.
The capacitor $C_1$ holds the charge while $CLK_1$ is ON and the capacitor $C_2$ holds the charge while $CLK_2$ is ON. The amplifier brings the input level to proper output stage. The amplifier should provide moderate gain and high frequency as low gain and low frequency affect the precision of the filter coefficient and results in inaccurate integration [30], [32], [33].

### 3.2.1 Theory of Operation

A SC integrator circuit performs the mathematical operation of integration; therefore, the output voltage is the response to the input voltage over time. In the $(n-1)^{th}$ clock period, while $CLK_1$ is high, from time $t_{n-1} = ((n - 1) \cdot T)$ to $t_{n-1/2} = ((n - 1/2) \cdot T)$, the capacitor $C_1$ is charged up to $V_{in} ((n - 1) \cdot T)$, i.e., the input voltage to the circuit at the time $((n - 1) \cdot T)$. Fig. 2.5 (a) shows the configuration of the SC integrator during $CLK_1$ [29].

The charge transfer of $C_1$ at $t_{n-1} = (n - 1) \cdot T$ is equal to the capacitance value multiplied by the voltage across the capacitor, as expressed in:

$$Q_{C_1} ((n - 1) \cdot T) = C_1 \cdot V_{in} ((n - 1) \cdot T)$$

(3.7)

where $T = 1/f$ is the period of non-overlapping clocks [29].
As soon as $CLK_2$ is on its rising edge, from time $t_{\frac{n-1}{2}} = ((n - 1/2) \cdot T)$ to $t_n = n \cdot T$, $C_1$ is discharged and the discharging current of $C_1$ passes through $C_2$. Fig. 3.5(b) shows the configuration of the SC integrator while $CLK_2$ is on its rising edge. The amount of charge of $C_2$ at $t_{\frac{n-1}{2}} = ((n - 1/2) \cdot T)$ is equal to the charge transfer from $C_1$ in addition to the previous amount of charge of $C_2$. Eq. (3.8) shows the amount of charge of $C_2$ at $t_{\frac{n-1}{2}} = ((n - 1/2) \cdot T)$.

$$Q_{C_2}((n - 1/2) \cdot T) = C_1 \cdot V_{in} ((n - 1) \cdot T) + C_2 \cdot V_{out} ((n - 1) \cdot T)$$  \hspace{1cm} (3.8)

The positive sign between two terms in Eq. (3.8) indicates that the SC integrator is a non-inverting integrator. Non-inverting SC integrators are insensitive to parasitic capacitances [30].

![Figure 3.5: Switched-capacitor integrator circuit during clock phases: (a) $CLK_1$, (b) $CLK_2$.](image)

Since $Q_{C_2}((n - 1/2) \cdot T) = C_2 \cdot V_{out} ((n - 1/2) \cdot T)$, the Eq. (3.8) is equal to:

$$C_2 \cdot V_{out} ((n - 1/2) \cdot T) = C_1 \cdot V_{in} ((n - 1) \cdot T) + C_2 \cdot V_{out} ((n - 1) \cdot T)$$  \hspace{1cm} (3.9)

Furthermore, as $V_{out}$ from $t_{\frac{n-1}{2}} = ((n - 1/2) \cdot T)$ to $t_n = n \cdot T$ is invariable, $V_{out} ((n - 1/2) \cdot T)$ can be substituted by $V_{out} (n \cdot T)$. Therefore Eq. (3.9) is changed to:
\[ V_{out} (n \cdot T) = \frac{c_1}{c_2} \cdot V_{in} ((n - 1) \cdot T) + V_{out} ((n - 1) \cdot T) \] (3.10)

For a small period, \( dV_{out} (t) \) can be substituted for \( V_{out} (n \cdot T) - V_{out} ((n - 1) \cdot T) \) and \( dt \) is equal to \( T \). As a result, Eq. (3.10) will be equal to Eq. (3.11) or Eq. (3.12).

\[
\frac{dV_{out} (t)}{dt} = f \cdot \frac{c_1 \cdot V_{in} (t)}{c_2} 
\] (3.11)

\[
V_{out} (t) = \frac{c_1}{c_2} \cdot f \cdot \int V_{in} (t) \, dt \] (3.12)

Thus, it is found that the circuit acts as an integrator [29] where the output voltage \( V_{out} \) is directly proportional to the clock frequency \( f \), the capacitance of the sampling capacitor \( C_1 \), and the integral of the input voltage \( V_{in} \). In addition, \( V_{out} \) is inversely proportional to the capacitance of the integration capacitor \( C_2 \).

### 3.3 Summary

This chapter introduced the Actel Fusion mixed-signal FPGA device and its key features and IP core devices; specifically, the configurable analog interface and the programmable timer. This chapter also presented the analysis of the SC integrator circuit and described the theory of the operation of this circuit.
Chapter 4: Proposed Design

In this chapter we introduce the our design goal, discuss our methodology for energy monitoring system, present the complete IP core architecture of the Actel Fusion mixed-signal FPGA device to interface energy measurement circuit and high-level software program application, and describe our proposed energy measurement circuit. Further, we detail our design analysis and review our design constraints.

4.1 Design Goal

The previous researches [2], [3], [4], [5], [6], [7], [8] show that there is a need for an accurate energy monitoring system to profile the energy consumption of software program applications for security, battery and energy management purposes. The goal of our design is to implement a high-precision energy monitoring system capable of measuring in real-time the energy dissipation of the device at the instruction level. We used the Actel Fusion mixed-signal FPGA device as a target testing platform for the core architecture. The Fusion device already integrates other analog components such as ADC. We implemented an energy measurement circuit that can be integrated as an analog IP core into a SoC design. The energy measurement circuit accumulates the voltage which is proportional to the current of the target device at fixed sampling intervals.

4.2 Methodology

The block diagram of the proposed energy monitoring system [34] is shown in Fig. 4.1. The mixed-signal FPGA device which is an Actel Fusion device samples the voltage and the current of the embedded device through $A_{V3}$ and $A_{C3}$ channels at fixed sampling intervals.
The voltage signal sampled from $A_{V3}$ is the supply voltage ($V_{DD}$) of the embedded device, and the current signal sampled from $A_{C3}$ is the measured current through the Actel Fusion external resistor ($R_{Actel}$). The fixed sampling interval is dependent on the frequency of the Fusion device, the ADC conversion time and the number of the instructions executed by the Cortex-M1 processor in each sampling cycle (the size of the code). However, as the frequency of the measurement from the ADC block is considerably low due to the software and hardware limitations, the current measurement of the target device will be lost between the sampling intervals. To address this, we implemented an energy measurement circuit to accommodate the low measurement rate of the Fusion device. The energy measurement circuit operates as a current integrator and accumulates the current of the target device within each sampling interval. This process
avoids loss of the current information and results in a more accurate energy estimation. To measure the instantaneous current of the device, the differential voltage across the energy resistor \( R_{energy} \) was monitored. This voltage is applied to the energy measurement circuit to be integrated at fixed sampling intervals. Since the variation of voltage within each sampling interval is insignificant [9], integration of the current is sufficient to calculate the instantaneous energy consumed by the device \( E = \int V \cdot I \cdot dt \).

The output voltage of the energy measurement circuit (i.e., proportional to the instantaneous energy) is fed into the Fusion device through \( A_{V2} \) channel to be processed by the Fusion device. After each sampling interval, the Fusion device sends a reset pulse signal to the energy measurement circuit and a new monitoring cycle is started. A connection to high-level software application is established through the CoreUART on-chip module.

**4.3 IP Core Architecture of the Actel Fusion Mixed-Signal FPGA Device**

The main reasons for choosing the Actel Fusion mixed-signal FPGA device for our proposed energy monitoring system is its low-power characteristics, its mixed-signal capabilities, and its suitability for applications targeting power management [18]. The design was implemented into the Fusion Embedded Development Kit Evaluation Board with a M1AFS1500 chip in the FGG484 package from Actel Company [35]. The main board components that are used in our design include two USB cables, a mixed-signal header connector and a miniature low-cost programming stick (LCPS). The USB cables are used for board powering up purposes as well as making the USB to UART connection to the host system. The mixed-signal header connector consists of the analog and the digital I/O pins. Through this connector different daughter boards can be connected to the evaluation board to verify various applications. Furthermore, the at-
tached low-cost programming stick (LCPS) is compatible with FlashPro programming software and enables programming the M1AFS1500-FGG484 device through the JTAG pins [35].

We developed the hardware IP core architecture of the Fusion device as well as its software application program. The combination of which allows the Fusion device to measure the current, the voltage and the energy of the target device at fixed sampling rates.

4.3.1 Actel Fusion Hardware Design

For Actel Fusion hardware design, Libero Integrated Development Environment (IDE) (version 9.1) was used as a main tool [18] to add the IP cores around the Cortex-M1 processor to design the entire system. Libero IDE includes SmartDesign tool which allows easy instantiation and connection of the Fusion IP cores to implement a Cortex-M1 system architecture. The goal was to design a hardware-based interrupt system to allow the Cortex-M1 processor to interact with the CoreAI in a cyclic way in order to perform the required measurements. Fig. 4.2 presents the block diagram of our hardware IP cores configuration.

As shown in Fig. 4.2, the Cortex-M1 processor shares CoreAHBLite with the high-speed IP core devices such as memory interfaces (i.e., CoreAhbNVM, CoreAhbSRAM and CoreMemctrl) and AHB-APB Bridge (i.e., CoreAHB2APB). CoreAHBLite connected Cortex-M1 as a master while it implemented CoreAhbNVM, CoreAhbSRAM, CoreMemctrl and CoreAHB2APB as slaves. CoreAHB2APB is a master for CoreAPB and ensures connections between the bus interfaces (i.e., CoreAHBLite and CoreAPB). CoreAPB interfaces the low-speed IP core devices; specifically, CoreAI, CoreGPIO, CoreUART and CoreTimer as slaves.
While CoreAI was instantiated, the corresponding analog quads of the sampling channels were configured. The sampling channels can be summarized as follows:

- $A_{V2}$ is connected to analog quad 2 which is set up to measure the voltage generated by the energy measurement circuit. Details regarding the function and operation of the energy measurement circuit will be discussed in the next subsection.

- $A_{V3}$ is connected to analog quad 3 which is set up to measure the supply voltage of the device at any monitoring point.

- $A_{C3}$ is connected to analog quad 3 which is set up to measure the current of the target device.
Since the voltage signal sampled from $A_{V2}$ is the output voltage of the energy measurement circuit, analog quad 2 was enabled to monitor voltage sources up to 4 V. This range was selected based on the supply voltage ($V_{DD}$) of the energy measurement circuit. Moreover, as the voltage signal sampled from $A_{V3}$ and the current signal sampled from $A_{C3}$ are, respectively, the supply voltage and the measured current of the embedded device, analog quad 3 was enabled to monitor voltage sources up to 4 V as well. This range was selected based on the supply voltage of the target device (usually less than 4 V) and also by considering the maximum measurable current of the target device, the resistance of the external sense resistor and the amplification factor of the Fusion built-in differential amplifier. In this design, the maximum measurable current was chosen to be 400 mA, and the value for $R_{Actel}$ was 0.5 Ω to reflect the maximum measurable current. In addition, the analog interface amplifies the current signal 10 times [18].

In this hardware-based interrupt system design there is not more than one interrupt; therefore, instantiation of CoreInterrupt is not significant. In fact, CoreTimer was connected directly to the Cortex-M1 processor’s interrupt signal (i.e., $IRQ_0$) and interrupts the processor at a defined period.

The system clock was utilized by the conjunction of the analog PLL and the RC oscillator. PLL generates the system clock and takes its input from the on-chip 100 MHz RC oscillator. In this design, Cortex-M1 runs up to 20 MHz and the system clock frequency is set by dividing 100 MHz by factor 5 in the PLL divider. Normally, the analog interface reference clock is derived from the system clock; however, in this design since PLL can provide more than one independent clock and in order to minimize the conversion time, the secondary clock is derived from PLL. This clock has a frequency of 40 MHz and it was only fed to the analog interface in
order to speed up the operation of the ADC. Additionally, this design contains one Actel macro, which is a 2-input AND gate. This macro keeps the system in reset mode until PLL generates the clock signal.

   SmartDesign tool was used to perform the required connections between the design entries (i.e., IP core devices, clock resources and Actel macros) and configure the system memory map. Fig. 4.3 presents the implemented hardware platform on Libero’s SmartDesign canvas.

   In addition to SmartDesign tool, Libero IDE introduces Synplify Pro tool to synthesize the design as well as physical implementation tools to perform place-and-route, compile, layout and timing analysis. Finally, the Fusion device architecture configured through a programming device such as low-cost programming stick (LCPS) by using the FlashPro tool.

   4.3.2 Actel Fusion Software Design

   The software application was implemented in the Actel SoftConsole IDE (version 3.3) tool in C programming language interface to implement the required features of the energy monitoring system targeting the architecture developed in subsection 4.2. The software application program configuration should support the SoC hardware configuration. The key feature of the application program is the integration of CoreTimer to interrupt the ARM Cortex-M1 processor at a defined period in order to access CoreAI voltage, current and energy measurement of the embedded device. The basic diagram for the measurement cycle program is depicted in Fig. 4.4.
Figure 4.3: Implemented hardware platform of IP cores connection on the SmartDesign canvas.
Figure 4.4: Basic diagram for the measurement cycle program.

The program operation is initiated by initializing the IP cores; specifically, CoreGPIO, CoreAI, CoreUART and CoreTimer. Initialization of CoreTimer causes its decrementing counter to start decreasing. When the counter reaches zero, an interrupt is generated. Since continuous mode is selected, the timer will be loaded automatically with the load value. Generation of the
interrupt moves the control of the program to an interrupt handler sub-routine. The interrupt handler subroutine disables all external interrupts and calls the CoreAI round-robin sub-routine. The CoreAI round-robin sub-routine first verifies the ADC statues to ensure the ADC is not busy sampling or converting. Second, it finds the next channel that requires sampling, and third it initiates the ADC cycle (i.e., sampling, distribution and post-calibration phases). Note that the ADC samples the channels sequentially; therefore, within a regular cycle we need to accommodate all channels that need sampling. In our implementation, we sample $A_{v2}$, $A_{v3}$, $A_{c3}$.

Prior to the initiation of the sampling, distribution and post-calibration phases, the ADC’s inputs such as mode, TVC and STC are configured. In this design, the ADC operates in the 12-bits mode and TVC and STC are set to 0 and 3.5, respectively, in order to ensure the minimum conversion time is met [18]. Next, the CHNUMBER [4:0] input, which selects one input channel for each ADC cycle, is loaded to the control register. While the ADC samples the analog channel (sampling phase), the status signals, SAMPLE and BUSY, go high. The SAMPLE signal goes low in distribution phase, however, the BUSY signal remains high indicating that the ADC is busy and converting the analog signal. The BUSY signal remains high during post-calibration phase to ensure ADC consistency. Once the conversion is complete the BUSY signal goes low and DATAVALID signal goes high specifying the corresponding digital result is available to read. The DATAVALID signal remains high until the next ADC cycle is started. The ADC assigns the digitized results to a specified array and passes the updated array as a parameter to the main routine. The main routine determines the type of the selected sampled channel, i.e., current or voltage. When the sampled channel is current, the measured current is reflected by the voltage drop across the external sense resistor, $R_{\text{Actel}}$; therefore, the result obtained from the ADC should be transformed to the current of the target device (see Eq. (3.1)). The result (digital value)
is transmitted to the high-level application module through CoreUART. Finally, the interrupt_enable function enables the interrupt for the next cycle.

The combination between hardware and software design of the Fusion device allows the measurement of the current and the voltage of the target device over the fixed sampling intervals. The duration of the sampling interval includes the time of conversion plus the time needed to execute the remainder of the program instructions required to process the sampled data. As a result, energy information will be lost within the sampling interval. Depending on the clock frequency of the targeted embedded device and the overall frequency cycle of the Fusion device, a large number of processor instructions can be executed during this interval on the targeted device. This, however, is unacceptable for both security and power management purposes. Also, sampling the power consumption at fixed intervals will reduce the overall precision of the energy measurement. In order to address these issues, there is a need for an energy measurement circuit to compensate for the Fusion low sampling rate. Hence, we implemented an energy measurement circuit capable of integrating the instantaneous current of the device and storing the integration information for each interval.

4.4 Proposed Energy Measurement Circuit

Fig. 4.5 shows the proposed energy measurement circuit. The aim is to accumulate the measured currents between the Fusion’s sampling intervals in order to compensate for the Fusion’s low sampling rate. Ideally, it is desirable to have an energy measurement circuit which is simple and offers the possibility to be implemented as an analog IP core on the Fusion device. The Fusion device already integrates an analog interface; therefore the integration of energy measurement circuit should be feasible. The challenge arises in reducing the complexity of the energy measurement circuit without sacrificing its accuracy.
As illustrated in Fig. 4.5, the energy measurement circuit comprises a conventional SC integrator, a pair of non-overlapping clocks, a differential amplifier, a reset circuit and a simple low-pass filter. The conventional SC integrator circuit contains four MOS switches and two capacitors. It integrates the input voltage over time by charging and discharging the capacitors when switches are open or closed. The SC integrator circuit uses NMOS transistors (M1, M2, M3 and M4) as switches where the gate terminal manages the state of the switch, and the source terminal and the drain terminal transmit the transferred charge. The sampling capacitor (C1) and the integration capacitor (C2) are used as storage elements while the input voltage is sampled or integrated. The pair of non-overlapping clocks controls the sampling and the integration operations. The integrated voltage is fed into a differential amplifier in order to bring the output voltage (Vout) to a proper input level required by the Fusion device. The reset block, which is composed of an n-channel transistor (M5) and a reset pulse, resets the circuit periodically. The resistor-capacitor (RC) low-pass filter is the last part of the output stage of the energy measurement circuit.
circuit that is used for the noise attenuation. This passive filter is a series connection of a resistor (R) with a capacitor (C₃). The output voltage is taken from the junction of these components (R and C₃).

The energy measurement circuit is designed, implemented and tested through various simulations in Cadence 65 nm CMOS process. Since the main concerns in SoC circuit design are accuracy and chip area optimization, the major emphasis of this design is on accuracy and chip area.

4.5 Design Analysis

In order to obtain accurate results from the energy measurement circuit, the components of the circuit should be analyzed in detail. Therefore, the following subsections focus on design specifications and trade-offs as well as brief descriptions of SC integrator’s auxiliary circuits, (i.e., non-overlapping clocks and differential amplifier).

4.5.1 Design Specifications

The maximum input voltage is a key design parameter. The maximum input voltage is derived from the maximum measurable current of the target device. In this design, the maximum measurable current was chosen as 400 mA. This current also dictates the constraints for our energy resistor (R_{energy}) and for the sizing of our differential amplifier. In our design, R_{energy} is set to a low value of 0.25 Ω in order to reduce power dissipation and supply voltage fluctuation. Therefore, the maximum input voltage is calculated as 100 mV.

The supply voltage is an additional design factor. Typically in nanoscale technology there is a tendency toward low supply voltages. However, since the supply voltage of the energy measurement circuit should be compatible with the internal reference voltage of the Fusion device
(\(V_{\text{ref}} = 2.56\,\text{V}\)), in this design a 2.5 V supply voltage was chosen. For this reason, high voltage MOS transistors were modeled as switches. These transistors were nch_25 models from the Taiwan Semiconductor Manufacturing Company 65 nm (tsmcN65) library. All the transistors are implemented as minimum size in order to minimize area of the design. In addition, minimum size transistors decrease charge injection and clock feed-through error [36]. The minimum width for nch_25 model transistors in the tsmcN65 library is 400 nm and the minimum length for NMOS transistors in this library is 280 nm (\(W_{\text{NMOS}} = 400\,\text{nm}, L = 280\,\text{nm}\)).

In the SC integrator circuit, the capacitance ratio \((C_1 / C_2)\) is another key design issue [30], [36]. The sampling capacitance, \(C_1\), should be small enough to charge up in half of the clock period. On the other hand, \(C_1\) cannot be so small that the parasitic capacitances will dominate and influence the circuit performance [36]. Moreover, according to Eq. (3.12) the capacitance ratio requires to be less than 1 \(((C_1 / C_2) < 1)\) in order to ensure that the SC integrator circuit does not saturate over the sampling interval. Therefore, the integration capacitance should be larger than the sampling capacitance. We determined through simulations that the integration capacitance, \(C_2\), should be at least six times greater than the sampling capacitance, so that the integration operation is accurate. Based on the input voltage range, the saturation conditions and the capacitor integration area trade-off, \(C_1\) and \(C_2\) were chosen to be 1 pF and 6 pF, respectively.

**4.5.2 Clock Generation Circuit**

There are numerous techniques for generating a pair of non-overlapping clocks [37]. The standard method is to generate the pair of non-overlapping clocks from a single clock [30]. The schematic of the clock generation circuit is shown in Fig. 4.6. This circuit is simple and consists of two main NOR gates and two cross-coupled inverter chains for creating non-overlap delay. In
this design, since the capacitors are small and they charge up rapidly, a shorter non-overlapping time is sufficient to avoid charge losses in the energy measurement circuit.

![Non-overlapping clock generation schematic](image)

**Figure 4.6: Non-overlapping clock generation schematic (the transistor level schematic is shown in Appendix).**

The non-overlapping clocks were arranged to guarantee that \( CLK_1 \) and \( CLK_2 \) are not high at the same time while they are running at the same frequency. It is preferable to have a higher frequency for non-overlapping clocks in order to increase the number of the samples over each Fusion monitoring interval. However, the higher frequency results in higher integration current which causes faster charge movement that saturates the circuit more rapidly. Increase of integration current also will result in more power dissipation. Therefore, the clock frequency of 1 MHz (\( T = 1 \mu s \)), with the pulse duration of 498 ns and rise and fall times of 1 ns, was applied based on the above mentioned conditions and the following relationship:

\[
T \gg R_{ON} \cdot C
\]  

(4.1)

The time constant \( T \) is determined by the ON resistance (\( R_{ON} \)) of the transistors and the value of the capacitors (i.e., \( C_1 \) and \( C_2 \)). The \( R_{ON} \) for the unit-size transistor in the standard library is typically several kilohms [31] and the values of the capacitors were chosen 1 pF and
Therefore, $T$ is on the order of tens of nanosecond. The transistors also contain parasitic capacitances in femto-farad range which are small enough to be neglected.

### 4.5.3 CMOS Differential Amplifier

The differential amplifier is a key building block in a SC integrator circuit as the amplifier gain directly affects the integration accuracy [33] and the amplifier’s power consumption is a significant factor of the total power consumption of the SC integrator circuit [36]. The general requirements for the differential amplifier as a part of the output stage of the SC integrator circuit is that it should contain a moderate dc gain with a unity-gain frequency at least five times faster than the clock frequency and phase margin greater than 70 degree [30]. These requirements can be satisfied by using the p-channel single-stage differential amplifier depicted in Fig. 4.7.

The advantage of the chosen amplifier is that it uses less silicon circuit area and provides moderate gain, high unity-gain frequency and negligible load. This differential amplifier uses n-channel transistors, $M_6$ and $M_7$, to form the differential pairs and p-channel transistors, $M_8$ and $M_9$, as a current mirror load. Transistor $M_{10}$ is a bias transistor where its gate is connected to a corresponding bias voltage. The bias voltage ($V_{bias}$) is built by using an n-channel transistor fed by a reference current.
Figure 4.7: CMOS differential amplifier using a p-channel current-mirror load (the detailed schematic is shown in Appendix).

Transistors $M_6$ and $M_7$ are biased by the drain current of the transistor $M_{10}$ ($I_{D10}$). These devices ($M_6$ and $M_7$) turn on by drawing part of the current $I_{D10}$, and in turn they will turn on $M_8$ and $M_9$. Therefore, under perfect symmetry all devices, $M_6$ to $M_9$, carry equal currents (i.e., $I_{D10}/2$). We designed all these devices to operate in saturation mode. The bias current is chosen so as to guarantee that all the devices are in saturation region while it minimizes the amplifier power consumption. The ideal voltage sources, $V_1$ and $V_2$, which are connected to the gates of $M_7$ and $M_6$, respectively, rise the bias voltage of these transistors to force these devices to operate in saturation region. In addition, we designed the transistors with minimum length and width, however, the aspect ratio of the PMOS transistors is twice larger than NMOS transistors due to PMOS transistors lower mobility.
Since all transistors operate in saturation region, the output swing of our particular differential amplifier is given by:

\begin{align}
V_{DS6} & \geq V_{GS6} - V_{TN} \implies V_{out} - V_{S6} \geq V_2 - V_{S6} - V_{TN} \implies V_{out} \geq V_2 - V_{TN} \quad (4.2) \\
V_{SD8} & \geq V_{SG8} - |V_{TP}| \implies V_{DD} - V_{out} \geq V_{SG8} - |V_{TP}| \implies V_{out} \leq V_{DD} - V_{SG8} + |V_{TP}| \quad (4.3)
\end{align}

Eq. (4.2) shows the amplifier’s minimum output voltage and Eq. (4.3) shows amplifier’s maximum output voltage with zero differential signal applied ($V_{in1} = V_{in2} = 0$). However, the practical implementation rarely matches the ideal value [38]. The output swing of the differential amplifier defines the limit of the output swing of the energy measurement circuit. Therefore, if the output swing of the energy measurement circuit exceeds the output swing of the differential amplifier, the measurement will saturate.

### 4.6 Design Constraints

The design of the energy measurement circuit is governed by constraints related to circuit saturation and noise reduction. In this section, these constraints are addressed and the associated design components justified.

#### 4.6.1 Circuit Saturation

One of the important considerations in designing a SC integrator circuit is circuit saturation, since integration is no longer valid following saturation. The time to saturation is dependent on the input voltage, the ratio of the capacitors and the clock frequency. Our experiments showed that for our design, the integration is accurate up to 90 μs, after which the circuit is fully saturated. Therefore, the circuit needs to reset before 90 μs in order to prevent saturation impact and maintain integration accuracy. To address this constraint, as it is shown in Fig. 4.5, we added a simple reset circuit to our energy measurement circuit which is composed of a reset switch ($M_5$)
and a reset signal source. The period of reset pulse source is consistent with the Fusion’s sampling rate. The reset pulse duration should be short to prevent charge losses in the energy measurement circuit and obtain precise measurement.

4.6.2 Noise Reduction

An additional important design constraint in the SC integrator circuit is switching noise. The switching noise can impact integration results by being stored on the integration capacitor \( C_2 \), and by being amplified. During simulations, we observed switching noise with a frequency of 2 MHz; a frequency two times greater than the frequency of the clock. In order to overcome this issue, we introduced a simple first-order RC low-pass filter to the output stage of the energy measurement circuit (See Fig. 4.5). Such a circuit is simple and includes the series combination of one resistor \( R \) and one capacitor \( C_3 \). The time constant of the filter was determined based on the cut-off frequency \( f_c \) relation:

\[
 f_c = \frac{1}{2\pi RC_3}
\]  

Since \( f_c \) is 2 MHz and \( C_3 \) was chosen to be 1 pF, \( R \) was calculated to be 80 K\( \Omega \). The reason for choosing the capacitance of 1 pF for \( C_3 \) was that this capacitance should be significantly less than the integration capacitance \( C_2 \); otherwise, it will influence the integration operation.

4.7 Summary

In this chapter, the design procedure and the details of the energy monitoring system were explained. We developed the IP architecture of the Actel Fusion device around the Cortex-M1 IP soft core in order to support all our interfaces. Specifically, the designed architecture needs to interface with the custom energy measurement chip to collect measurements and with the securi-
ty and power management high-level software applications to transmit the measurements. The proposed methodology is to use the programmability and the flexibility of the Fusion device to sample the voltage and the current of the target device while accommodating its low sampling frequency by designing an energy measurement circuit. The energy measurement circuit was designed as a current integrator over a fixed interval using the SC integrator technique. This circuit stores the integration of the current over sampling intervals. Table 4.1 summarizes the design specifications of the energy measurement circuit.

**Table 4.1: Design specifications**

<table>
<thead>
<tr>
<th>Specifications</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>65 nm CMOS</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>2.5 V</td>
</tr>
<tr>
<td>Maximum measurable current</td>
<td>400 mA</td>
</tr>
<tr>
<td>Maximum input voltage</td>
<td>100 mV</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>1 MHz</td>
</tr>
<tr>
<td>Sampling capacitance</td>
<td>1 pF</td>
</tr>
<tr>
<td>Integration capacitance</td>
<td>6 pF</td>
</tr>
<tr>
<td>Transistors dimensions</td>
<td>( w_{\text{NMOS}} ) (nm) = 400, ( w_{\text{PMOS}} ) (nm) = 800, ( l ) (nm) = 280</td>
</tr>
</tbody>
</table>
Chapter 5: Results and Discussion

This chapter presents simulation and experimental results used to verify the functionality and performance of the proposed energy monitoring system. First, a simple method is described to verify the accuracy of our Fusion hardware and software design and to estimate the Fusion’s sampling rate. Then, the differential amplifier as a main building block of energy measurement circuit is studied. Next, the overall performance of the energy measurement circuit is validated through the running of several simulations. Finally, the comparison of the simulation results to the ideal results is provided. This comparison formulates the relationship between the energy measurement circuit results and the mathematical integration results (i.e., ideal results).

5.1 Experimental Results of Actel Fusion mixed-signal FPGA

This section presents the Fusion’s experimental results in order to provide a functional reference for the designed energy measurement circuit. Experimentally, the average sampling error was calculated and also the maximum frequency of the operation for our Fusion simulation based on our custom design was measured. For the experiment, we used a simple setup presented in Fig. 5.1. This experimental setup is composed of a signal generator (BK Precision 4040A), a measurement board, an Actel Fusion Embedded Development Kit Evaluation Board and a host system.
The target device was modeled by using a waveform generated by the signal generator which is a square waveform with duty-cycle of 50 percent and a frequency of $10 \text{ kHz}$ ($T =$
100 μs). The amplitude of the square waveform was set to 1 V. This waveform was applied to one of the existing pins on the measurement board (i.e., the corresponding pin to channel \( A_{V2} \)). Although, the Fusion hardware architecture and software application program are set to sample three channels \( (A_{V2}, A_{V3}, A_{C3}) \), in this setup and for experimental purposes, only channel \( A_{V2} \) is connected to the square waveform voltage source with the remaining analog channels \( (A_{V3} \text{ and } A_{C3}) \) left floating.

The measurement board containing the current sensor \( (R_{Actel}) \) was connected to the evaluation board through the J10 mixed-signal header connector. The evaluation board includes a M1AFS1500 Fusion FPGA device which was used to implement the hardware-based interrupt system in order to sample the analog channel \( A_{V2} \) at fixed sampling rate. The evaluation board was connected to the host system through the USB port. The host system contains high-level software application. The system clock is synchronized by a 20MHz clock signal generated by PLL and RC oscillator. The reference clock for the analog interface is also derived from PLL and RC oscillator and is set to 40 MHz.

While the Fusion program application was executing, 500 successive measurements were collected on the host system. The sampled results were analyzed with MATLAB. Of these samples 166 samples are associated to channel \( A_{V2} \) since the design is assigned to three sampling channels. These 166 samples must go through cycles of 0s and 1s. However, the analysis of results indicated that the amplitude of the sampled results is not precisely fixed at 1 V. This in turn introduces sampling error. This error was calculated and the average error was estimated to be 3% ± 3 (it is believed that this error is mainly due to measurement setup).
To estimate the overall sampling rate of the Fusion device, the number of the successive 0s and the number of successive 1s in 166 samples of channel $A_{V2}$ were considered. These numbers demonstrate the number of samples per signal level we achieved while the square waveform is high or low. For this experiment it is assumed that the channel $A_{V2}$ sample results greater than 800 mV are equal to 1 V, and the samples results less than 200 mV are equal to 0 V. For simplicity, the sample results between these values were ignored. According to the analysis in each period of square waveform while the square waveform is high, the host computer receives 3 to 4 successive 1s. Similarly, while the square waveform is low, the host computer receives 3 to 4 successive 0s. Overall, the host computer receives 7 samples in each period and therefore the overall sampling rate of the Fusion device is calculated at 14.2857 $\mu$s. This sampling rate is rounded up to 15 $\mu$s to ensure that there is enough time for sampling the selected channels ($A_{V2}$, $A_{V3}$ and $A_{C3}$). Fig. 5.2 presents the sampled voltage results for three periods of the square waveform.

![Sampled voltage for three periods of the inputted square waveform.](image)

**Figure 5.2: Sampled voltage for three periods of the inputted square waveform.**
Therefore, 5 µs is a minimum rate for sampling each channel, given that our design was set up for sampling three channels. Table 5.1 shows the Fusion timing performances for the implemented design obtained with a 40 MHz analog interface clock frequency and 12-bits ADC mode. TVC and STC also are fixed at 0 and 3.5, respectively, to satisfy the minimum conversion time. Additionally, the time for ADC to operate reading and writing commands is assumed as the worst case, which is equivalent to the period of the analog interface clock. Therefore, whole conversion time, $T_{\text{conv}}$, of one analog input is equal to 2 µs. In addition to conversion time, the design includes a low number of instructions which must be executed in order to perform desired measurements. Since the system clock frequency is 20 MHz, 3 µs provides adequate time to execute approximately 60 instructions.

<table>
<thead>
<tr>
<th>Timing performances</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC sampling time</td>
<td>0.55 µs</td>
</tr>
<tr>
<td>ADC distribution time</td>
<td>1.2 µs</td>
</tr>
<tr>
<td>ADC post-calibration time</td>
<td>0.2 µs</td>
</tr>
<tr>
<td>ADC read time</td>
<td>0.025 µs</td>
</tr>
<tr>
<td>ADC write time</td>
<td>0.025 µs</td>
</tr>
<tr>
<td>Total ADC conversion time</td>
<td>2 µs</td>
</tr>
<tr>
<td>Program instructions execution Time</td>
<td>3 µs</td>
</tr>
<tr>
<td>Total Sampling Rate per Channel</td>
<td>5 µs</td>
</tr>
</tbody>
</table>

**5.2 Circuit Simulation Results**

The proposed energy measurement circuit was designed and simulated in Cadence using 65 nm CMOS technology with a 2.5 V supply voltage. First, the response of the differential amplifier was studied improving the precision of the energy measurement circuit. Then, the integration
operation was verified by looking at the transient analysis of the energy measurement circuit. Finally, we compared our energy measurement circuit results to the ideal results obtained from the Cadence built-in calculator, defined their relationship and derived the associated constants (energy conversion constants). The validation and optimization of these constants were explored through running various simulations. All simulations were performed by using Spectre circuit simulator.

5.2.1 Analysis of CMOS Differential Amplifier

The differential amplifier is a key building block of the SC integrator as it improves the precision of integration. The performance of the differential amplifier, shown in Fig. 4.7, was characterized by general design specification, voltage transfer curve, maximum output voltage, frequency response and total power consumption.

5.2.1.1 General Design Specifications

To design an amplifier, the general design specifications include transistors size, threshold voltage, region of operations and bias current. To optimize the chip area, in this design all MOS transistors were set to the minimum length of 280 nm, with a minimum width of 400 nm for NMOS transistors and a width of 800 nm for PMOS transistors. The threshold voltages for NMOS and PMOS transistors of this technology are 0.515 V and −0.418 V, respectively. All transistors operate in saturation region and the bias current is set to 100 µA in order to reduce the amplifier power consumption.

5.2.1.2 Voltage Transfer Curve

The voltage transfer curve of the differential amplifier is explored in order to assign the proper values to the voltage sources $V_1$ and $V_2$ to guarantee that all transistors operate in saturat-
tion region and the amplifier provides high gain. Fig. 5.3 plots the voltage curve while the differential-mode input \((V_1 - V_2)\) has been swept from \(-1\) to \(+1\) V. As seen from the voltage transfer curve, the variation in differential-mode input voltage causes \(V_{out}\) swings toward ground or \(V_{DD}\).

While \(V_1\) is more negative than \(V_2\), \(M_7\) is OFF so as \(M_9\) and \(M_8\). Since no current flows from \(V_{DD}\), \(M_6\) and \(M_{10}\) operates in deep triode region and \(V_{out} = 0\). As \(V_1\) approaches \(V_2\), \(M_7\) turns on and a small current flows through \(M_7\) \((I_{D7})\) and eventually through \(M_9\) and \(M_8\). The small current in \(M_7\) implies a current increase in \(M_6\) \((I_{D6})\) since \(I_{D10} = I_{D6} + I_{D7}\). Therefore, \(I_{out}\) becomes negative and \(V_{out}\) is small. While \(V_1\) and \(V_2\) are adequately close, \(M_6\) and \(M_8\) are saturated and the differential amplifier provides high gain [28]. For this reason, we set \(V_1 = V_2 = 1\) V. With similar analysis, while \(V_1\) is more positive than \(V_2\), \(I_{out}\) becomes positive and \(V_{out}\) increases. Further increase in \(V_1\) turns \(M_6\) off, therefore \(M_8\) operates in deep triode region, and \(V_{out} = V_{DD}\).

![Figure 5.3: Voltage transfer curve for the differential amplifier of Fig. 4.7.](image)
5.2.1.3 Maximum Output Voltage

The maximum output voltage of the differential amplifier defines the maximum output of the energy measurement circuit. Therefore, if the maximum output voltage of the energy measurement circuit exceeds the maximum output voltage of the differential amplifier, the measurement will saturate. The maximum output voltage of the amplifier was studied by plotting the output voltage ($V_{out}$) curve versus the supply voltage ($V_{DD}$) while $V_{DD}$ has been swept from 0 to 2.5 V (Fig. 5.4). As shown in Fig. 5.4, for $V_{DD} < |V_{TP}|$, $V_{out} = 0$ and as $V_{DD}$ approaches 2.5 V the highest $V_{out}$ is found at $V_{DD} = |V_{GS9}|$.

![Graph showing the relationship between output voltage and supply voltage for the differential amplifier.](image)

**Figure 5.4: Maximum output voltage of the differential amplifier of Fig. 4.7**

5.2.1.4 Frequency Response

The frequency response of the differential amplifier presents a dc gain, a unity-gain frequency and a phase margin. The dc gain gives an indication of the accuracy of the differential amplifier, the unity-gain frequency determines the speed of the amplifier and the phase margin
measures the stability of the amplifier. The frequency response was found through AC analysis where an AC signal source was set as an input signal. The AC simulation is shown in Fig. 5.5. Since all transistors were set to a minimum length and minimized width, this results in a moderate dc gain of 20 dB. Using the minimum length and width for transistors optimizes the chip area; however, the trade-off is a lower dc gain. Fig. 5.5 also shows that the differential amplifier has a high unity-gain frequency of 5.37 GHz and an acceptable phase margin of 87°.

![Frequency Response](image)

**Figure 5.5:** Simulated dc gain, unity-gain frequency and phase margin of differential amplifier of Fig. 4.7.
5.2.1.5 Total Power Dissipation

The amplifier power dissipation is a significant factor of the total power consumption of the energy measurement circuit. In this design, the bias current was set to 100 μA and the supply voltage to 2.5 V, the total power dissipation of the differential amplifier, therefore, is 250 μW. Consequently, the energy measurement circuit can be considered a low-power circuit since this resulting power dissipation is negligible when compared to the total power dissipation of the portable devices. Table 5.2 summarizes the most important properties of the differential amplifier.

Table 5.2: Differential amplifier simulated results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{DD}</td>
<td>2.5 V</td>
</tr>
<tr>
<td>Minimum output voltage</td>
<td>0.485 V</td>
</tr>
<tr>
<td>Maximum output voltage</td>
<td>1.846 V</td>
</tr>
<tr>
<td>DC gain</td>
<td>20 dB</td>
</tr>
<tr>
<td>Unity-gain frequency</td>
<td>5.37 GHz</td>
</tr>
<tr>
<td>Phase margin</td>
<td>87°</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>250 μW</td>
</tr>
</tbody>
</table>

5.2.2 Transient Analysis Results of the Energy Measurement Circuit

The functionality of the energy measurement circuit as a current integrator was investigated by using transient analysis. The transient analysis was performed for various types of inputs. These included regular basic waveforms such as sine, pulse, sawtooth and ramp, and one irregular waveform. The maximum amplitude of these input waveforms did not exceed 100 mV, thereby satisfying the maximum current constraint for the target device. The details of these input waveforms and their integration output results are as follows:
- Sine: The period of the inputted sine waveform was chosen at 250 kHz to ensure the waveform is going through sampling and integration cycles in each Fusion monitoring interval. The amplitude is 45 mV with an offset voltage of 45 mV. The offset voltage is necessary since the energy measurement circuit is not designed for negative voltage values. Fig. 5.6 plots the input sine waveform and its integration output results.

Figure 5.6: Input sine waveform and its integration output results.
- Pulse: The applied input pulse waveform frequency is 4 µs with the pulse duration of 1.999 µs and the rise and the fall times were set to 500 ps. Fig. 5.7 presents the input pulse waveform and its integration output results.

**Figure 5.7: Input pulse waveform and its integration output results.**
- Sawtooth: The applied input sawtooth waveform frequency is 4 µs and the rise and the fall times were set to 2 µs. Fig. 5.8 presents the input pulse waveform and its integration output results.

![Sawtooth Waveform](image)

**Figure 5.8:** Input sawtooth waveform and its integration output results.
- Ramp: Fig. 5.9 depicts the input ramp waveform and its integration output results.

![Ramp Waveform Diagram](image)

**Figure 5.9:** Input ramp waveform and its integration output results.
- Irregular: Fig. 5.10 shows the input irregular waveform and its integration output results.

![Irregular Waveform](image)

**Figure 5.10: Input irregular waveform and its integration output results.**

As seen from the integration output results (i.e., Fig. 5.6, Fig. 5.7, Fig. 5.8, Fig. 5.9 and Fig. 5.10) the output goes through cycles of integration. The integration result is sampled every 15 µs by the Fusion device. After the sampling process, the Fusion device sends the reset pulse signal and a new integration cycle is initiated. Therefore, the energy measurement circuit accumulates the energy information between two successive sampling points of the Fusion device. Table 5.3 summarizes the integration results at each rest point.
Table 5.3: Integration results at each rest points

<table>
<thead>
<tr>
<th>Time (µs)</th>
<th>Sine</th>
<th>Pulse</th>
<th>Sawtooth</th>
<th>Ramp</th>
<th>Irregular</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 µs</td>
<td>0.64591931</td>
<td>0.64605905</td>
<td>0.64563344</td>
<td>0.6586316</td>
<td>0.61877336</td>
</tr>
<tr>
<td>30 µs</td>
<td>0.65103683</td>
<td>0.65340873</td>
<td>0.6492372</td>
<td>0.68124205</td>
<td>0.62229886</td>
</tr>
<tr>
<td>45 µs</td>
<td>0.64489663</td>
<td>0.64478171</td>
<td>0.64492399</td>
<td>0.7043618</td>
<td>0.68919652</td>
</tr>
<tr>
<td>60 µs</td>
<td>0.63980354</td>
<td>0.6374853</td>
<td>0.64133632</td>
<td>0.70765341</td>
<td>0.70208855</td>
</tr>
<tr>
<td>75 µs</td>
<td>0.6459193</td>
<td>0.64605952</td>
<td>0.64563344</td>
<td>0.69700741</td>
<td>0.7110081</td>
</tr>
<tr>
<td>90 µs</td>
<td>0.65103683</td>
<td>0.65340873</td>
<td>0.6492372</td>
<td>0.68646009</td>
<td>0.69799136</td>
</tr>
<tr>
<td>105 µs</td>
<td>0.64489663</td>
<td>0.64478171</td>
<td>0.64492399</td>
<td>0.67600543</td>
<td>0.66677666</td>
</tr>
<tr>
<td>120 µs</td>
<td>0.63980354</td>
<td>0.6374853</td>
<td>0.64133632</td>
<td>0.66567613</td>
<td>0.66972596</td>
</tr>
<tr>
<td>135 µs</td>
<td>0.6459193</td>
<td>0.64605952</td>
<td>0.64563344</td>
<td>0.65546396</td>
<td>0.65261775</td>
</tr>
<tr>
<td>150 µs</td>
<td>0.65103683</td>
<td>0.65340873</td>
<td>0.6492372</td>
<td>0.64537684</td>
<td>0.68116047</td>
</tr>
</tbody>
</table>

5.2.3 Energy Conversion Constants

As found in the previous subsection, the output of the energy measurement circuit is proportional to the integral of the input current over time. However, this output needs to be converted to represent an accurate energy measurement. Based on our experiments, we formulated two matrices in order to compare the circuit’s results (simulation results) with the ideal results (mathematical results). The integration results obtained from the circuit were collected in a circuit output matrix, while the ideal results calculated by the Cadence built-in calculator were stored in a calculator output matrix. The contents of these matrices were then analyzed through MATLAB to determine the relationship between the contents of two matrices. The analysis considered 1st, 2nd, 3rd and 4th order polynomial approximation functions. Part of MATLAB source code of the matrices’ relationship determination for input sine waveform is as follows:
%SINE

%Open traces file for output from schematic

sine_circuit_output_file = 'H:\sine_circuit_output.txt';
sine_circuit_output= load(sine_circuit_output_file);

%Open traces file for output from calculator

sine_calculator_output_file = 'H:\ sine_calculator_output.txt';
sine_calculator_output= load(sine_calculator_output_file);

%Finding relation between results from schematic and calculator

sine_first_order=polyfit(sine_circuit_output,sine_calculator_output,1);
sine_second_order =polyfit(sine_circuit_output,sine_calculator_output,2);
sine_third_order =polyfit(sine_circuit_output,sine_calculator_output,3);
sine_fourth_order =polyfit(sine_circuit_output,sine_calculator_output,4);

The MATLAB analysis indicated that the linear relationship (1st order approximation) provided the best fit. In order to convert circuit results to reflect the accurate measurement, the relation below must hold:

\[ K \cdot V_{out}(t) + A = \frac{C_1}{C_2} \cdot f \cdot \int V_{energy}(t) \, dt \]  \hspace{1cm} (5.1)

The constants \( K \) and \( A \) were called energy conversion constants. Using MATLAB, the energy conversion constants for all input waveforms were derived and are summarized in Table 5.4. Table 5.4 indicates that the variations of \( K \) and \( A \) for different input waveforms are all within a close range. Therefore, the constants can be assumed independent from the input waveform. The average values of \( K \) and \( A \), 1.2454 and −0.6914, respectively, were assumed as the final values. The final values are then used to convert the circuit results.
Table 5.4: Energy conversion constants \((K \text{ and } A)\) for each input waveform.

<table>
<thead>
<tr>
<th>Input Waveform</th>
<th>(K)</th>
<th>(A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sine</td>
<td>0.9034</td>
<td>-0.4702</td>
</tr>
<tr>
<td>Pulse</td>
<td>0.9928</td>
<td>-0.5277</td>
</tr>
<tr>
<td>Sawtooth</td>
<td>1.0086</td>
<td>-0.538</td>
</tr>
<tr>
<td>Ramp</td>
<td>1.6278</td>
<td>-0.9369</td>
</tr>
<tr>
<td>Irregular</td>
<td>1.6944</td>
<td>-0.9842</td>
</tr>
<tr>
<td>Average</td>
<td>1.2454</td>
<td>-0.6914</td>
</tr>
</tbody>
</table>

5.2.3.1 Validation of Energy Conversion Constants

In order to assess the precision of the final values of \(K\) and \(A\) (i.e., the average values), these constants were applied to the circuit output matrices, and the updated matrices were compared to the content of the calculator output matrices for various input waveforms. The validation testing compares the circuit results of the original input waveforms mentioned in Table 5.4 and tested \(K\) and \(A\) values for 3 new input waveforms. The new input waveforms were chosen as irregular waveforms. There were two reasons for choosing these irregular waveforms. First, the irregular waveforms best model the characteristics of the measured current signals of the target device. Second, these input waveforms are independent from the original \(K\) and \(A\) estimation; therefore their simulation results can validate the accuracy of the final values of \(K\) and \(A\) for the wider range of input waveforms. The irregular waveforms and their integration output results are depicted in Fig. 5.11, Fig. 5.12 and Fig. 5.13.
Figure 5.11: Input irregular1 waveform and its integration output results.

Figure 5.12: Input irregular2 waveform and its integration output results.
Figure 5.13: Input irregular3 waveform and its integration output results.

The percentage error for each input waveform was calculated through MATLAB. The part of MATLAB source code of error calculation for input sine waveform is as follows:

```matlab
%SINE
sine_updated_circuit_output = sine_circuit_output * K + A;

%Error Calculation
Error = ((sine_calculator_output - sine_updated_circuit_output) ./ sine_calculator_output) * 100;
absoluteValueOfError = abs(Error);
AverageError = mean(absoluteValueOfError);

%Standard deviation
StandardDeviation = std(absoluteValueOfError);
```
Table 5.5 summarizes the percentage error for each type of input waveform with $K$ and $A$ final values applied. Fig. 5.14 to Fig. 5.21 show the comparison among updated circuit output’s matrix and calculator output’s matrix for 10 points for each inputted waveform. The light colored portion of the bars shows the circuit output whereas the dark colored portion of the bars show the calculator output.

Table 5.5: Average error values for sine, pulse, ramp and irregular input waveforms

<table>
<thead>
<tr>
<th>Input Wave</th>
<th>Error Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sine</td>
<td>3% ± 2</td>
</tr>
<tr>
<td>Pulse</td>
<td>4% ± 2</td>
</tr>
<tr>
<td>Sawtooth</td>
<td>4% ± 3</td>
</tr>
<tr>
<td>Ramp</td>
<td>7% ± 4</td>
</tr>
<tr>
<td>Irregular</td>
<td>9% ± 3</td>
</tr>
<tr>
<td>Irregular1</td>
<td>8% ± 2</td>
</tr>
<tr>
<td>Irregular2</td>
<td>9% ± 2</td>
</tr>
<tr>
<td>Irregular3</td>
<td>9% ± 3</td>
</tr>
</tbody>
</table>
Figure 5.14: Comparison of sine waveform circuit and calculator output results.

Figure 5.15: Comparison of pulse waveform circuit and calculator output results.
Figure 5.16: Comparison of sawtooth waveform circuit and calculator output results.

Figure 5.17: Comparison of ramp waveform circuit and calculator output results.
Figure 5.18: Comparison of irregular waveform circuit and calculator output results.

Figure 5.19: Comparison of irregular1 waveform circuit and calculator output results.
According to Table 5.5, a maximum error of 9% ± 3 is obtained for the irregular input waveform while the regular sine input gives a much smaller error. It can be seen that the error is inversely proportional to the regularity of the input signal.
5.2.3.2 Optimization of Energy Conversion Constants for Irregular Waveforms

Given that the irregular waveforms best model the characteristics of the measured current signals of the target device, it merits optimizing the energy conversion constants for irregular waveforms. In order to optimize $K$ and $A$ values, the methodology applied in the previous subsection was repeated only for the irregular waveforms. Table 5.6 summarizes the associated $K$ and $A$ values for each irregular input waveform. The average values of $K$ and $A$ values (i.e., considered as final values) were obtained as 1.6516 and $-0.9539$, respectively. Table 5.7 summarizes the average of error with $K$ and $A$ values applied. Comparison between results summarized in Table 5.5 and Table 5.7 shows error reduction up to 7%.

Table 5.6: Energy conversion constants ($K$ and $A$) for irregular input waveforms.

<table>
<thead>
<tr>
<th>Input Waveform</th>
<th>$K$</th>
<th>$A$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Irregular</td>
<td>1.6944</td>
<td>-0.9842</td>
</tr>
<tr>
<td>Irregular1</td>
<td>1.6152</td>
<td>-0.9281</td>
</tr>
<tr>
<td>Irregular2</td>
<td>1.6585</td>
<td>-0.9586</td>
</tr>
<tr>
<td>Irregular3</td>
<td>1.6386</td>
<td>-0.9449</td>
</tr>
<tr>
<td>Average</td>
<td>1.6516</td>
<td>-0.9539</td>
</tr>
</tbody>
</table>

Table 5.7: Average error values for irregular input waveforms.

<table>
<thead>
<tr>
<th>Input Waveform</th>
<th>Error Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Irregular</td>
<td>4% ± 3</td>
</tr>
<tr>
<td>Irregular1</td>
<td>2% ± 1</td>
</tr>
<tr>
<td>Irregular2</td>
<td>3% ± 2</td>
</tr>
<tr>
<td>Irregular3</td>
<td>2% ±2</td>
</tr>
</tbody>
</table>
5.3 Summary

This chapter presented the results for verification of the functionality of the energy monitoring system. The experimental results of Actel Fusion mixed-signal FPGA device was presented to validate the accuracy of the design in order to sample the specific analog input signal and to estimate Fusion’s maximum sampling rate. Also, in order to show the accuracy of the proposed energy measurement circuit, the differential amplifier was first optimized, and then the functionality of the energy measurement circuit was investigated through transient analysis for several input waveforms. Finally, the simulation results of the energy measurement circuit were compared to the ideal results in order to formulate their relationship and compute the associated energy conversion constants. These energy conversion constants were validated through running various simulations.
Chapter 6: Conclusions and Future Work

In this dissertation, we presented FPGA-based solution for energy monitoring system composed of mixed-signal FPGA device and energy measurement circuit. We designed an energy measurement circuit that uses an SC integrator technique and outputs a voltage that is proportional to the integral of the instantaneous current consumption of an embedded device. The energy measurement circuit was implemented and simulated in 65 nm CMOS technology with a 2.5 V supply voltage. We designed the energy measurement circuit with total power dissipation of 250 µW. The proposed energy measurement circuit considerably minimizes the silicon area. It contains a few number of transistors (28 transistors in total) and each transistor has a length of 280 nm, and a width of 400 nm for NMOS and 800 nm for PMOS. In addition, the sampling capacitance and integration capacitance are 1 pF and 6 pF, respectively. Therefore, the major issue in the integrated circuit design, i.e., size of the design, is addressed. The simulation results gave an indication of high efficiency of the implemented energy measurement circuit for the accumulation of the current of the target device within the sampling intervals. Our simulation results showed that the energy measurement circuit can store the energy information no larger than 90 µs. Furthermore, we found that there is a linear relationship between the implemented energy measurement circuit results and the mathematical integration results (ideal results) calculated by Cadence built-in calculator. We derived the associated constants, $K$ and $A$, for energy conversion applications in order to achieve accurate measurement. By applying these energy conversion constants to the circuit output results, we determined that our circuit results have at most 9% ± 3 error in comparison to the ideal results when an irregular input signal is applied to the energy measurement circuit. This amount of error decreases with the regular input waveforms. We also
optimized the energy conversion constants for irregular waveforms as irregular waveforms are most representative of the current signals of the targeted embedded device. With optimization, the percentage of the error drops up to 7% for irregular waveforms, resulting in a maximum error of 4% + 3.

Furthermore, since the energy measurement circuit is a general-purpose circuit, it can be implemented along with any embedded device. Implementation of the energy measurement circuit within the embedded devices enables hardware-software co-design where energy measurement circuit samples the energy of the targeted embedded device at hardware level and high-level software application generates the real-time profile of the energy at software level. The hardware-software co-design is potentially a good trade-off between accuracy and speed. The profile of the energy can contain the information of the total energy or a fraction of the energy consumed by the device (i.e., various procedures within a program). This profile of the energy can be used for security, battery and energy management purposes.

Within the security domain, the profile of the energy is of interest in order to develop a countermeasure against PAA. The profile of the energy can be used along with software current flattening technique in order to determine the number and the places of NFIs to be inserted.

In battery management systems, the profile of the energy can estimate the power demands of the output load. The estimation of power demands of the output load in multi-battery and multi-cell systems can be used to select the most optimal scheduling charge and discharge algorithm. Also, the profile of the energy can warn the device in case of the battery overcharging.

For energy management purposes, the profile of the energy can be combined with DVS technique to assign suitable supply voltage levels to program applications (i.e., the lower supply
voltage level during the low computational periods and higher supply voltage level when re-
quired). Also, since the power peak regions are a critical threat to the reliability of the system as
they can lead to voltage drop and result in system error or system reset, the energy profile can
identify the periods of the power peaks within the software program application to assure the re-
liability of the system.

We used the mixed-signal FPGA as a target device for the core architecture. Our chosen
FPGA device is Fusion from Actel Company for its analog features and its programmability. The
focus was to make use of Fusion’s analog features (analog quads, analog multiplexer, ADC and
prescaler circuit) and its interrupt generator timer to interrupt the Cortex-M1 processor at fixed
sampling intervals in order to sample the voltage and the current of an embedded targeted device.
We designed the Fusion IP core architecture as well as its software program application to inte-
grate Cortex-M1 processor, configurable analog interface, programmable timer, bus interfaces
and clock circuitry resources. The experimental results validated the effectiveness of our Fusion
design for sampling the voltage, the current and the energy of the target device with the average
sampling error of 3% ± 3. This error is primarily due to measurement setup. The experimental
results further indicated that the Fusion device enables sampling the voltage, the current and the
energy of the target device at a minimum rate of 15 μs. This low sampling rate is due to the low
frequency of the Fusion’s ADC’s internal clock (i.e., limited up to 10 MHz).

6.1 Future Work

Future research and development can explore the possibility of fabricating the energy
measurement circuit in the TSMC 65nm CMOS technology. The fabricated circuit can be easily
integrated as an IP core within Actel Fusion mixed-signal FPGA device or any other mixed-
signal FPGA device that allows integration of analog components.
References


76


Publications

Appendix: Circuit Diagrams

In this appendix the schematics of the circuits implemented in Cadence are presented.

Figure A.1: Energy measurement circuit
Figure A.2: Non-overlapping clock generation schematic
Figure A.3: CMOS differential amplifier using a p-channel current-mirror load