Fully-Integrated Boost and Buck Converters with High Efficiency and Optimized Inductor Geometry

by

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Abstract

FULLY-INTEGRATED BOOST AND BUCK CONVERTERS WITH HIGH EFFICIENCY AND OPTIMIZED INDUCTOR GEOMETRY

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This thesis presents the modelling, design, and implementation of fully-integrated dc-dc converters. Since simple and accurate integrated inductor models for dc-dc converters are not currently available, the main objective of this thesis is to develop new models and compare the analysis, simulation, and measurement results of a proposed design. To achieve that, the circuit theory of both step-up and step-down converters is first presented in detail. The existing models, developments, and techniques in implementing fully integrated dc-dc converters are also highlighted. Complete mathematical models, which take the relevant losses into consideration for both the step-up and step-down converters, are developed next. A dedicated model for the integrated inductor that is tailored for power converters along with its parasitic resistance is also developed and presented. The proposed inductor model further optimizes the geometry without increasing the area; this consequently maximizes the performance of the inductor. Finally, an overall optimization algorithm combining both the converter and the inductor models is proposed and discussed in detail.
Several converter topologies with different inductor geometries are designed and compared. Two step-up and two step-down converters are designed, simulated and compared. Each set contained a circuit with a square inductor and a circuit with the proposed inductor geometry. A fast pulse-width-modulated control system is designed to regulate the converters. Simulation results are presented, demonstrating the improvements in performance and conversion efficiency of the converter based on the proposed inductor geometry over that of the square-inductor based converter. A good agreement between the analytical calculations and the simulated results is reported. A prototype containing the four converters was fabricated in a 65-nm digital CMOS process. The feasibility of fabricating efficient fully integrated dc-dc converters is demonstrated and recommendations for future research are given.
Dedicated to my parents
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<th>Full Form</th>
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<tr>
<td>AC</td>
<td>Alternating-Current</td>
</tr>
<tr>
<td>ASITIC</td>
<td>Analysis and Simulation of Spiral Inductors and Transformers for ICs</td>
</tr>
<tr>
<td>CAD</td>
<td>Computer-Aided Design</td>
</tr>
<tr>
<td>CCM</td>
<td>Continuous Conduction Mode</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal-Oxide-Semiconductor</td>
</tr>
<tr>
<td>DCM</td>
<td>Discontinuous Conduction Mode</td>
</tr>
<tr>
<td>DC</td>
<td>Direct-Current</td>
</tr>
<tr>
<td>DRC</td>
<td>Design Rule Check</td>
</tr>
<tr>
<td>EMI</td>
<td>Electromagnetic Interference</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>IoT</td>
<td>Internet of Things</td>
</tr>
<tr>
<td>ITRS</td>
<td>International Technology Roadmap for Semiconductors</td>
</tr>
<tr>
<td>LCD</td>
<td>Liquid-Crystal Display</td>
</tr>
<tr>
<td>LVS</td>
<td>Layout Versus Schematic</td>
</tr>
<tr>
<td>MIM</td>
<td>Metal-Insulator-Metal</td>
</tr>
<tr>
<td>MOM</td>
<td>Metal-Oxide-Metal</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal-Oxide-Semiconductor Field-Effect Transistor</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
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<tr>
<td>--------------</td>
<td>------------------------------------------------</td>
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<tr>
<td>MOS</td>
<td>Metal-Oxide-Silicon</td>
</tr>
<tr>
<td>NMOS</td>
<td>N-channel Metal-Oxide-Semiconductor</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>PEX</td>
<td>Parasitic Extraction</td>
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<tr>
<td>PFM</td>
<td>Pulse Frequency Modulation</td>
</tr>
<tr>
<td>PMOS</td>
<td>P-channel Metal-Oxide-Semiconductor</td>
</tr>
<tr>
<td>PTC</td>
<td>Positive Temperature Coefficient</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse Width Modulation</td>
</tr>
<tr>
<td>SEPIC</td>
<td>Single-Ended Primary-Inductor Converter</td>
</tr>
<tr>
<td>SRAM</td>
<td>Static Random-Access Memory</td>
</tr>
<tr>
<td>TSMC</td>
<td>Taiwan Semiconductor Manufacturing Company</td>
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Chapter 1

Introduction

1.1 Motivations

It is envisioned that the Internet of Things (IoT) will make our world greener: wireless sensor networks will detect pollution; smart grids will support the use of renewable sources; precision agriculture will save water and minimize the use of chemicals; self-driving vehicles will reduce the fuel consumption, etc. The IoT is a global network infrastructure composed of a large number of devices that are equipped with microcontrollers, transceivers, and suitable protocols that make them able to communicate with one another [1]. The promise of the IoT is to optimize the use of available resources as the global population grows, while simultaneously improving the quality of services, reducing the operational costs, and protecting the environment [2]. However, the web of billions of sensors and online nodes that underpins the IoT concept might also be detrimental to the environment due to the energy used by the devices and the communication infrastructure and the data centres driving them, and because of the manufacturing and disposal of the associated components.

For the reasons above, the challenges facing electronic engineers due to power dissipation and high integration are greater today than they have ever been. Cramming more elements together into a smaller volume leads to power densities high enough to cause silicon to fracture. Accordingly, the International Technology Roadmap for Semiconductors (ITRS) has identified power as a long-term grand challenge as an exponential increase in power dissipation over the next decade is forecasted. At the same time, the impact of the energy challenge is amplified by the worldwide spread of portable, wearable, sensor, and IoT devices (e.g. the information and communication technology contribution to greenhouse emissions is around 2% today and will increase to 6%–8% in 2020 [3]).
At the heart of every electronic device lies a power management unit that is responsible for optimizing the power that the device uses in different conditions. The introduction of power semiconductors and power MOSFETs (Metal-Oxide Semiconductor Field-Effect Transistors) \cite{4}, made it feasible to develop circuits that convert a direct-current (dc) voltage to a different level dc voltage without having to convert it to alternating-current (ac) first. The main component of a power management unit is the dc-dc converter, a circuit that steps up or down a supply voltage as shown in Fig. 1.1. In a microsystem in order for the supply side to provide power to the computing (processing, memory) or interfacing sides (transceivers, sensors, speakers, displays, etc.), dc-dc converters have to be in between to provide the optimized power level for the intended application. Different techniques to convert dc to dc exist including: linear converters, capacitive converters, and inductive converters. Inductive converters are the most commonly used converters since they provide higher efficiencies and larger output currents \cite{5-7}. Besides the high efficiency requirement, dc-dc converters for portable, wearable, sensor, and IoT devices are also subject to stringent size, weight, and cost constraints. Existing discrete converters use multiple off-chip components, which adds to the cost, size, and complexity to these devices. Integrating all the elements of a converter on chip was proposed to address some of these challenges \cite{8-14}.

With full integration comes another set of challenges resulting from the different functions...
including digital, analog, and radio-frequency circuits coexisting on a single chip. The power
dissipation of digital circuits is reduced by scaling down the supply voltage; however, noise-
dominated analog circuits require specific voltage levels (e.g. sensor readouts, memories, and
transceivers). This challenge is accentuated further for IoT devices for three main reasons:
energy, compactness, and compatibility. Since IoT devices will be deployed everywhere in large
numbers, the converters need to use little energy to operate. Not only will they need to be able
to harvest and use ambient energy that is otherwise wasted but also should be able to store it and
use it when an ambient source is not available. Finally, the converters of the IoT devices will
also have to be small and light enough to be integrated seamlessly and scaled to large numbers
without adding size or cost to the unit device. Those converters need to be compatible with
the existing technology, power levels, protocols, and infrastructure for a seamless integration to
occur. All of these functions have to be offered without adding more volume, weight, cost, or
power to the miniaturized IoT devices.

1.2 Objectives and methods

The main component of a dc-dc converter is the inductor, which is implemented as a planar
connection of a number of metal segments. These metal segments introduce parasitic resistances
which have a dramatic effect on the conversion efficiency since they cause significant energy
losses. Moreover, since the planar inductor occupies most of the converter’s area, optimizing the
inductor not only improves the conversion efficiency but also contributes to optimizing the area
occupation.

In order to address the previously-mentioned challenges, accurately modelling monolithic dc-
dc converters is essential. Inductive dc-dc converters have been studied extensively. Monolithic
converters on the other hand are less investigated in the literature. Therefore, the first objective of
this work is to study and compare different existing models and introduce a model that is tailored
for fully integrated boost converters. This paves the way for obtaining a relationship between the
conversion efficiency and different power losses, which assists in improving performance.

The second objective is to study the integrated inductor along with its parasitic resistances.
The inductance of integrated inductors has been previously modelled \cite{15-19}. Integrated induc-
tors come in different geometrical shapes. Based on those shapes, the inductance and the parasitic
resistance change. The parasitic resistance sets a maximum bound to the allowable inductance
based on area and frequency constraints. Therefore, accurately modelling the parasitic resistance
of an inductor in a given metal layer is crucial in optimizing the inductance time-constant ratio.
In this thesis a conformal mapping model is used to calculate the value of the resistance \cite{20}.
Thus, arriving at a complete model for integrated inductors based on the geometrical shape.
The third objective is finding a trade-off of the inductance versus the parasitic resistance for a given set of specifications (i.e. shape, area, fabrication technology, frequency). This trade-off provides the points where the inductance time-constant ratio is maximized. It is also necessary to relate the parameters of the dc-dc converter to those of the integrated inductor in order to arrive at an algorithm that optimizes the conversion efficiency based on a given set of specifications. The optimization algorithm is useful to develop design guidelines for a specific technology, and to quickly assess the performance of dc-dc converters without having to perform full-scale simulations. The algorithm also allows the designer to have a first estimate of the overall design parameters therefore reducing the design time.

The fourth objective is to design step-up and step-down converters along with the appropriate control schemes for a 65-nm process. Finally, the circuits are fabricated and characterized to evaluate their functionality and performance. The 65-nm process was chosen since it is a standard digital/mixed signal process that is well established and used in numerous applications. Additionally, it offers a thick top metal layer that is appropriate for designing inductors.

Proper methods and tools need to be applied to successfully design and implement the proposed circuits. First, behavioural models are established in computer algebra programs and analog modelling languages and used as design guidelines/limits. An inductor design and simulation software is used for designing and characterizing integrated inductors in addition to the software developed to import inductors for drafting. Electronic design automation tool suite is used for schematic designs and circuit simulations. After optimizing the schematic design and meeting the specifications, the chip layout was drafted and the performance compared to that of the circuit schematic for validation.

1.3 Contributions

The work presented here provides modelling, analysis, optimization, design, and implementation guidelines to enable successful integration of boost and buck dc-dc converters. Two boost converter circuits and two buck converter circuits were designed and fabricated in a TSMC 65-nm process. The aim of this work is to develop approaches to increase the conversion efficiency while optimizing the use of the silicon area available. Design trade-offs are also discussed to allow the designer to make decisions based on the given specifications.

The main contributions of this thesis are summarized as follows:

- A model for fully integrated boost and buck converters that considers both conduction losses and switching losses.
• Parasitic resistance calculation formula that takes the corners of a given shape into consideration and uses the Schwarz–Christoffel transformation.

• A shape factor \( k \) that describes an inductor shape and ranges from 0 (square) to 1 (regular octagon).

• A software application that takes geometrical specifications and generates files to be readily used in ASITIC for inductor analysis and in Virtuoso Layout Editor in Cadence for drafting the layout of the inductor.

• An inductance time-constant optimization algorithm for a given inductor area and frequency.

• Different boost converter topologies developed: dual-inductor converter, coupled-inductor converter, and parallel-coupled-inductor converter.

• A test chip with the proposed boost and buck converters and control circuits is implemented in the TSMC 65-nm technology.

1.4 Thesis organization

The thesis is organized to present the analyses, designs, implementations, tests, and results of the proposed converters.

Chapter 2 provides a general background on different types of power converters. Linear regulators and switched-mode regulators are both introduced with more emphasis on the switched-mode type. Since inductive regulators are the main focus of this work, buck and boost converters are discussed in more detail.

Chapter 3 models both boost and buck dc-dc converter and provides the important definitions. It also provides an overview of the theory of operation in both conduction modes.

Chapter 4 is dedicated to modelling the integrated inductors. The lumped-element electrical model is first introduced with the relevant elements highlighted, followed by the expression used to calculate the inductance of an integrated inductor.

Using the simple model of Chapter 2, a model that takes both the conduction losses and the switching losses along with all the main component non-idealities for each converter is discussed in Chapter 5. This chapter also explores the losses related to integrating the different elements of a converter and derives a design model.
Chapter 6 models the resistance of corners which is a relevant challenge when dealing with integrated inductors. The resistance of corners is calculated using the Schwarz–Christoffel transformation depending on the shape of the inductor.

Chapter 7 optimizes the inductance time-constant ratio. The chapter starts by analyzing the relationship between the conversion efficiency of a boost converter and the inductance time-constant ratio of an inductor. The geometrical parameters of an inductor are also studied to show their effect on the inductance time-constant ratio. A shape factor $k$ is introduced to describe different shape and is optimized to achieve the highest inductance time-constant ratio.

Chapter 8 discusses the different topologies considered at the design stage of the boost converter and compares their conversion efficiencies. This chapter also introduces pulse-width-modulation and pulse-frequency-modulation schemes and their use in controlling fully-integrated boost converters.

Chapter 9 presents the implementation of the designed circuits. The different blocks are introduced along with the functioning of each. The simulation results of the four converters designed are also reported in this chapter along with comparisons to the results reported in the literature.

Chapter 10 concludes the thesis with the discussion of the obtained results and future developments.

Finally, Appendix A shows the papers published to disseminate this work.
Chapter 2

Voltage regulators background

In this chapter, the power converter background is presented. Different types of voltage regulators are introduced in Section 2.1 with more emphasis on inductive dc-dc regulators. Linear regulators are discussed in Section 2.2 and capacitive converters in Section 2.3. Analysis of different topologies are then introduced in Section 2.4.

2.1 Voltage regulators classification

Different power supply technologies have been developed and improved over the years allowing advances in electronic circuits of all kinds. Many electronic systems require multiple supply voltages to operate. A power supply is defined as a constant voltage source with a high current capability. A regulated power supply is one which maintains an output voltage within a narrow range, regardless of line voltage, load current, and temperature variations.

As shown in Fig. 2.1, voltage regulators come in two main categories: linear regulators and switched-mode regulators [21]. Linear regulators consist of series and shunt voltage regulators. Traditionally, linear regulators were commonly used due to their low electromagnetic interference (EMI) noise, excellent load and line regulation, ease of integration and low area overhead. However, they can only step down the input voltage and their efficiency is limited by the ratio of the input to the output voltage. With the growing difference between digital supply voltages and the off-chip battery voltage, linear regulators have become less optimal [5,6].

The two main classes of switched-mode regulators are: switched-capacitor regulators and inductive regulators. Unlike linear regulators, switched-mode dc-dc converters utilize energy-storing elements and switches to permute the connections between the input and the output.
Capacitive converters (also known as charge pumps) use only capacitors as energy-storing elements and can provide reasonable efficiencies for large voltage differences. However, capacitive converters can only provide low current loads \[22,23\]. The peak efficiency of a capacitive converter is limited by its output resistance, which is a function of the switching frequency and the capacitance. Consequently, the efficiency increases as the load current decreases which limits the converter usability. Typical efficiencies are lower than 80% for reasonable capacitance sizes \[5,24\].

Inductive dc-dc converters (regulators) consist of one or more inductors and capacitors and at least two switches.\[1\] Inductive converters can be pulse-width modulated, pulse-frequency modulated, or a combination of the two. Unlike linear and switched-capacitor regulators, inductive regulators have efficiencies that depend solely on the parasitics of their components, and as a result they can usually achieve efficiencies in the range of 80-95% \[21\]. Inductive dc-dc converters are the focus of this work.

Switched regulators in general, provide high efficiencies, high power densities, and can have multiple output levels. However, they have slow response to load and line changes, produce high levels of EMI noise and have high output ripple.

### 2.2 Linear regulators

A dc-dc converter is a device that takes an unregulated dc input voltage $V_{IN}$ and converts it into a regulated output voltage $V_{OUT}$ that has a magnitude or a phase (or both) which are different from those of the input voltage. The ratio of $V_{OUT}$ to $V_{IN}$ is defined as the voltage conversion ratio.

\[1\] Off-chip dc-dc converters usually use one switch and one freewheeling diode.
When the conversion ratio is greater than one the converter is said to step-up the input voltage, and when it is smaller than one, the converter is the step-down type.

Linear regulators were first introduced to overcome the efficiency and the regulation problems of a power supply. The efficiency problem is due to the fact that when a supply voltage is to be stepped down by a resistive divider, power is lost in the dropping resistor and depending on the ratio of the output voltage to the supply this is over 50% of loss. The regulation problems stems from the fact that it is rare for a primary source to be absolutely constant, and voltage fluctuations could cause severe functional problems for the load. Therefore, a control scheme must be introduced by which the output voltage is measured and the supplied energy is varied according to the requirements of the load. If the source voltage decreases, the controller must increase the source current to prevent a decrease in the output voltage.

Linear regulators make use of an amplifier, a reference voltage, and a resistor to control the current supplied to the load as shown in Fig. 2.2. The resistance of the $M_1$ is set by the error voltage produced by the amplifier. Resistors $R_{f1}$ and $R_{f2}$ copy a scaled version of the output voltage $V_{OUT}$ which is compared to the reference voltage $V_{REF}$ which sets the value of the output voltage

$$V_{OUT} = V_{REF} \frac{R_{f1}}{R_{f2}}.$$  \hfill (2.1)

The linear regulator effectively solves the regulation problem; however the efficiency problem still exists. Additionally, the output voltage can only be lower than input voltage.
2.3 Capacitive converters

Unlike linear voltage converters, switched-mode converters can generate an output voltage that is higher than the input voltage. A capacitive dc-dc converter (charge pump) typically steps up a supply voltage to an output voltage that is multiple times higher. Charge pumps consist of only capacitors and switches which makes integration easier in comparison to inductive converters [25]. Charge pumps were originally used in smart power ICs and non-volatile memories [26], more recently, they have been used in voltage regulators, SRAM, and LCD drivers [27]. An ideal one-stage charge pump is shown in Fig. 2.3, which consists of a voltage source $V_{IN}$, two switches, $S_1$ and $S_2$ driven by two complementary clock signals, a pumping capacitor $C$ and a load which comprises $C_L$ and $I_L$. The pumping capacitor is connected to a clock signal $V_{CLK}$ with an amplitude equal to the voltage source as shown in Fig. 2.4. During the first phase (0 to $T/2$), $S_1$ is closed and $S_2$ is open, and $V_{CLK}$ is zero which connects one terminal of $C$ to ground and the other to $V_{IN}$. This charges $C$ to $V_{IN}$ while $V_{OUT}$ is discharged by the current load $I_L$ for a charge
of $I_L T/2$. In the second phase ($T/2$ to $T$) the clock signal is high, therefore, part of the charge stored in $C$ is transferred to the load capacitor $C_L$ and a charge of $I_L T/2$ to the current load. The output voltage will increase at each cycle until reaches the asymptotic steady state value of

$$V_{OUT} = 2V_{IN} - \frac{I_L T}{C}.$$ (2.2)

Several cycles are required to approach the asymptotic value and the step increment of the output voltage in each step gets smaller. Therefore, using a one stage charge pump the output voltage can be boosted up to an ideal value that is twice the power supply, not including the losses due to the current load [28]. A common limitation of charge pumps is the fact that the conversion efficiency reaches a maximum a certain value of voltage gain. In applications when the voltage gain needs to the variable charge pumps are not preferred.

## 2.4 Inductive converters

Unlike capacitive dc-dc converters, inductive dc-dc converters use an inductor instead of a capacitor. Inductive converters come in various structures based on the number of switches, isolation and function. The single-ended converters are the step-up and step-down converters which produce an output voltage higher or lower than the input voltage, respectively. Various other types exist such as: buck-boost, Čuk, forward, flyback, full-bridge, and single-ended primary input converter (SEPIC) [21]. Performance of dc-dc converters can be evaluated based on conversion efficiency, voltage ripple, and load and line regulation. Conversion efficiency is one of the most important performance metrics. For discrete high-power converters, it is used to determine the amount of dissipated power in the form of heat. For monolithic low-power converters, conversion efficiency is used to determine their feasibility since they usually use limited battery resources [5].

### 2.4.1 General structure

A general block diagram of a dc-dc converter with a negative feedback network is shown in Fig. 2.5. It consists of four main parts: a dc-dc converter block, which is the power stage that produces an output voltage $V_{OUT}$ that is higher or lower than an input voltage $V_{IN}$, a constant voltage $V_{REF}$ which is a constant voltage usually produced by a bandgap reference circuit, a feedback network which takes a fraction of the output voltage to be compared with $V_{REF}$, and a control circuit that
compares the resistive divider voltage to the constant $V_{REF}$ producing an amplified error voltage which is in turn used to control the dc-dc converter switches in order to keep $V_{OUT}$ constant.

When a certain power $P_{IN}$ is delivered to the input of a dc-dc converter, a portion of this power, $P_{OUT}$, is transferred to its load. An ideal converter would have equal input and output powers, since all its components would be ideal and hence have no power losses. Practical converters, on the other hand, would dissipate a portion of the input power, $P_{LOSS}$, in the form of heat. The power balance of a dc-dc converter is depicted in Fig. 2.6.
2.4.2 Main topologies

A dc voltage is usually obtained from a rectified ac line or a battery. In this work the main concern is battery-operated applications, since they have more strict constraints on power, area, and cost. Due to these constraints, most applications contain only a single battery which provides a single supply voltage. The two main topologies are discussed next.

**Step-Down converters**

In applications powered by Lithium-ion batteries, with a typical cell voltage of 3.7 V, the battery voltage needs to be stepped-down for some blocks on the chip. For instance, digital blocks and signal processing circuits need lower supply voltages in order for the consumed power to be minimized. Traditionally, step-down dc-dc converters were implemented with off-chip components. The converter consisted of a chip for the control system, and external passive components (inductors and capacitors) and power switches. The whole converter would then be connected to the application chip which added overhead to the packaging, mounting, and overall printed circuit board (PCB) area.

Having all the passive external components, power switches, and control circuitry integrated on the same chip is essential, especially as the constraints on cost, battery run-time, and weight get tighter. Fully-integrated step-down converters have been more evident in the literature in comparison to step-up converters [6, 12, 29–32] with efficiencies ranging from 45% to 78%.

**Step-Up converters**

In numerous situations the input voltage supplied to the system is insufficient. When the input voltage is supplied by an energy harvesting device or a Nickel Metal-Hydride battery, which has a typical cell voltage of 1.2 V, most analog blocks on the chip will be unable to operate properly. For example, line-drivers or power amplifiers, typically require a higher supply voltage in order to be able to transmit data into a communication channel [5].

As discussed in the previous section, integrating all elements on chip is crucial, however, it comes with a cost of low conversion efficiencies. Reported efficiencies are in the range of 20% to 40% [5, 9, 33]. Thus far monolithic step-up dc-dc converters have not been commercially available. The main reason is the lack of complete dedicated models for fully integrated converters, which include modelling the on-chip inductor along with its parasitics, optimizing the inductance per parasitic resistance value and hence optimizing the overall efficiency. To achieve this, a clear understanding of the differences between discrete dc-dc converters and their integrated...
counterclockwise is required. Additionally, the issues that come with the integration of passives, high switching frequencies, and control techniques have to be taken into account.

For the reasons listed above, monolithic step-up dc-dc converters are the main focus of this work. The basic theory and modes of operation for ideal step-up dc-dc converters are discussed in detail in the next section.

2.5 Summary

In this chapter the general background on different types of voltage regulators was introduced in the first section. Linear regulators were briefly discussed in the second section. Charge pumps were introduced in section three. The main focus of the work is inductive dc-dc converters, which were discussed in more detail in the fourth section.
Chapter 3

Theory of operation of step-up and step-down converters

This chapter offers an overview of the analysis and modelling of both step-up and step-down dc-dc converters. The circuit structure and theory of operation of boost converters are discussed in Section 3.1. Both conduction modes are also presented and analyzed. The circuit structure and theory of operation of buck converters are discussed in Section 3.2.

3.1 Structure of ideal step-up dc-dc converters

A dc-dc converter can be modelled in several ways. The most common approach is to analyze the converter’s voltage and current waveforms and construct a system of equations to describe its behaviour. In order to build the basis for this work, a simplified ideal model is discussed in this section [5], [21].

The analysis to follow for both converter types assumes that:

• All the converter components are ideal and lossless.
• All the passive component are linear, time-invariant, and frequency-independent.
• Switching losses are zero.
• All currents and voltages are linearized.
The converter operates in steady state.

Fig. 3.1 shows the schematic of a step-up (boost) dc-dc converter, in which the output voltage \( V_{OUT} \) is higher than the input voltage \( V_{IN} \). The converter consists of an inductor \( L \), two switches \( S_1 \) and \( S_2 \) controlled by intervals \( \Phi_1 \) and \( \Phi_2 \), respectively, a filter capacitor \( C \), and a load resistor \( R \). Switches \( S_1 \) and \( S_2 \) are switched at a clock frequency \( f_{SW} = 1/T \), with duty cycle, \( D \), defined as the time when \( S_1 \) is on divided by the time interval \( T \). A boost dc-dc converter can operate in two conduction modes: the continuous conduction mode (CCM), and the discontinuous conduction mode (DCM). In CCM the steady-state current through the inductor \( i_L(t) \) has a positive value. On the other hand, in DCM, \( i_L(t) \) varies between a positive value and zero (i.e. the inductor current does not flow continuously).

### 3.1.1 Continuous conduction mode

A boost converter in CCM works in two phases. The equivalent circuits of both phases are shown in Fig. 3.2. The first phase is bound by the time interval \( 0 < t \leq DT \), where \( \phi_1 \) is high and \( \phi_2 \) is low, resulting in \( S_1 \) being on and \( S_2 \) being off, respectively. The voltage across the inductor \( v_L \) is equal to the input voltage \( V_{IN} \), therefore, the inductor is charged by the voltage source causing the inductor current \( i_L(t) \) to increase from its minimum value \( I_{L_{min}} \) to its maximum value \( I_{L_{max}} \) with a slope of \( V_{IN}/L \), at the same time the filter capacitor discharges through the load as shown in Fig. 3.2(a).

The second phase starts at time \( t = DT \) and lasts until the end of the period \( T \), in this phase, \( \phi_1 \) is low and \( \phi_2 \) is high, hence, \( S_1 \) is off and \( S_2 \) is on. The inductor starts acting as a current...
source and gets discharged into the filter capacitor and the load. The voltage across the inductor, \( v_L \), becomes equal to \( V_{IN} - V_{OUT} \). The inductor current \( i_L(t) \) decreases from its maximum value \( I_{L_{max}} \) to its minimum value \( I_{L_{min}} \) with a slope of \( (V_{IN} - V_{OUT})/L \). Since \( L \) is discharged in series with the input voltage \( V_{IN} \), the output voltage \( V_{OUT} \) of the boost converter is always higher than its input voltage for steady-state operation.

**Phase 1**

The first phase starts when switch \( S_1 \) closes and switch \( S_2 \) opens. The current through \( S_2 \) is zero and the voltage across it is \(-V_{OUT}\). The voltage across \( S_1 \) is zero. The linearized voltage across the inductor \( L \) in phase 1 is shown in Fig. 3.3 and is given by

\[
 v_L(t) = V_{IN} = L \frac{di_L}{dt},
\]  

(3.1)
The inductor charges in this phase with a current $i_L(t)$ which is equal to the current in $S_1$ in phase 1 and is expressed as

$$i_L(t) = i_{S1}(t) = \frac{1}{L} \int_0^t v_L \, dt + i_L(0) = \frac{1}{L} \int_0^t V_{IN} \, dt + i_L(0) = \frac{V_{IN}}{L} t + i_L(0),$$

where $i_L(0)$ is the minimum (initial) current at $t = 0$. The maximum (peak) inductor current is then given by

$$i_L(DT) = \frac{V_{IN} DT}{L} + i_L(0).$$

The inductor current $i_L(t)$, $S_1$ current $i_{S1}(t)$, and $S_2$ current $i_{S2}(t)$ in phase 1 are shown in Figs. 3.4 to 3.6 respectively.

This phase ends at $t = DT$, when $S_1$ is turned off, and $S_2$ is turned on.

**Phase 2**

The second phase starts when switch $S_1$ opens and switch $S_2$ closes. The current through $S_1$ is zero and the voltage across it is $V_{OUT}$. The voltage across $S_2$ is zero. The linearized voltage across the inductor $L$ in phase 2 is shown in Fig. 3.3 and is given by
CHAPTER 3. THEORY OF OPERATION OF STEP-UP AND STEP-DOWN CONVERTERS

Figure 3.4: The linearized current through the inductor, $i_L(t)$, in CCM.

Figure 3.5: The linearized current through $S_1$, $i_{S1}(t)$, in CCM.

Figure 3.6: The linearized current through $S_2$, $i_{S2}(t)$, in CCM.
\[ v_L(t) = V_{IN} - V_{OUT} = L \frac{di_L}{dt}, \] (3.4)

which is less than zero, indicating that \( V_{IN} < V_{OUT} \).

The inductor discharges in this phase with a current \( i_L(t) \) which is also equal to the current in \( S_2 \) in phase 2 and is found to be

\[ i_L(t) = i_{S2}(t) = \frac{1}{L} \int_{DT}^{t} v_L \, dt + i_L(DT) = \frac{1}{L} \int_{DT}^{t} (V_{IN} - V_{OUT}) \, dt + i_L(DT) = \frac{V_{IN} - V_{OUT}}{L} (t - DT) + i_L(DT), \] (3.5)

where \( i_L(DT) \) is the maximum (peak) current at \( t = DT \). The inductor current at the end of this phase \( i_L(T) \) is equal to the minimum (initial) current \( i_L(0) \).

This phase ends at the end of the period when \( t = T \) when \( S_2 \) is turned off and \( S_1 \) is turned on again.

**Voltage gain**

The average voltage value across the inductor in steady state using the volt-second balance is

\[ V_L = \frac{1}{T} \int_{0}^{T} v_L \, dt = 0. \] (3.6)

From Fig. 3.3 this can be expressed as

\[ V_{IN}DT = (V_{OUT} - V_{IN})(1 - D)T \Rightarrow V_{OUT} = \frac{V_{IN}}{1 - D}. \] (3.7)

It follows that the ratio between the dc output voltage, \( V_{OUT} \), and the dc input voltage, \( V_{IN} \), for an ideal converter is

\[ M = \frac{V_{OUT}}{V_{IN}} = \frac{I_{IN}}{I_{OUT}} = \frac{1}{1 - D}. \] (3.8)

where \( I_{IN} \) and \( I_{OUT} \) are the average input and output currents, respectively. It should also be noted that for an ideal converter \( 1 < M < +\infty \).
At this point it is relevant to calculate the peak-to-peak inductor current as a function of the duty cycle $D$ since inductors and switches are usually characterized by the maximum current rating (stress), which is the maximum current a device can continuously carry while remaining within its temperature rating. From (3.2), (3.3), and (3.7), the peak-to-peak value of the inductor current $\Delta i_L$ is then

$$\Delta i_L = i_L(DT) - i_L(0) = \frac{V_{IN} DT}{L} - \frac{V_{IN} D}{L f_{SW}} = \frac{V_{OUT} D(1 - D)}{L f_{SW}}.$$  \hfill (3.9)

Taking the derivative of $\Delta i_L$ relative to the duty cycle $D$ for constant $V_{OUT}$, $L$, and $f_{SW}$

$$\frac{d\Delta i_L}{dD} = \frac{V_{OUT}}{f_{SW} L} (1 - 2D),$$  \hfill (3.10)

Setting the derivative to zero, the maximum value of $\Delta i_L$ occurs at $D = 0.5$ and is expressed by

$$\Delta i_{Lmax} = \frac{V_{OUT}}{4 f_{SW} L}.$$  \hfill (3.11)

The peak switch current (for both $S_1$ and $S_2$) is given by

$$I_{S1max} = I_{S2max} = I_{IN} + \frac{\Delta i_{Lmax}}{2}.$$  \hfill (3.12)

Since the converter is assumed to be ideal, the input power $P_{IN}$ is equal to the output power $P_{OUT}$. Consequently, the conversion efficiency $\eta$ is 100%.

$$\eta = \frac{P_{OUT}}{P_{IN}}.$$  \hfill (3.13)

### 3.1.2 Discontinuous conduction mode

Unlike in CCM, a boost converter in DCM works in three phases. The equivalent circuits are shown in Fig. 3.7. The first phase starts at $t = 0$ and ends at $t = DT$. During this phase, $\phi_1$ is high ($S_1$ is on) and $\phi_2$ is low ($S_2$ is off). The voltage across the inductor $v_L$ is equal to the input voltage $V_{IN}$ and therefore, the inductor is charged by the voltage source causing the inductor current $i_L(t)$ to increase from its minimum value $I_{Lmin} = 0$ to its maximum value $I_{Lmax}$ with a slope of $V_{IN}/L$, at the same time the filter capacitor discharges through the load as shown in Fig. 3.7(a).
The second phase, shown in Fig. 3.7(b), starts at time $t = DT$ and ends at time $t = (D + D_1)T$, where $D_1$ is the time at which $S_2$ is on divided by the total period $T$. In this phase, $S_1$ is off and $S_2$ is on. The inductor starts acting as a current source and gets discharged into the filter capacitor and the load. The voltage across the inductor becomes $v_L$ which is equal to $V_{IN} - V_{OUT}$. The inductor current $i_L(t)$ decreases from its maximum value $I_{Lmax}$ to zero with a slope of $(V_{IN} - V_{OUT})/L$.

The last phase starts at time $t = (D + D_1)T$ and ends at $t = T$. Both switches are off in this phase, thus the current through the inductor becomes zero, making the voltage across it equal to zero. The equivalent circuit is shown in Fig. 3.7(c).

**Phase 1**

During this time interval $S_1$ is on and $S_2$ is off, the voltage across $S_1$ is zero, the voltage across $S_2$ is $-V_{OUT}$, and the voltage across the inductor is shown in Fig. 3.8 and is given by

$$v_L(t) = V_{IN} = L \frac{di_L}{dt}, \quad i_L(0) = 0.$$ (3.14)

The inductor current is equal to the $S_1$ current and is given by

$$i_L(t) = i_{S1}(t) = \frac{1}{L} \int_0^t v_L \, dt + i_L(0) = \frac{1}{L} \int_0^t V_{IN} \, dt + 0 = \frac{V_{IN}}{L} t,$$ (3.15)

The peak inductor current which is equal to $\Delta i_L$ in DCM is then given by

$$i_L(DT) = \Delta i_L = \frac{V_{IN} DT}{L} = \frac{V_{IN} D}{L f_{SW}}.$$ (3.16)

This phase ends when $S_1$ turns off and $S_2$ turns on.

**Phase 2**

The second phase starts when switch $S_1$ opens and switch $S_2$ closes. The current across $S_1$ is then zero and the voltage across it is $V_{OUT}$. The voltage across $S_2$ is zero. The linearized voltage across the inductor $L$ in phase 2 is shown in Fig. 3.8 and is given by

$$v_L(t) = V_{IN} - V_{OUT} = L \frac{di_L}{dt} < 0.$$ (3.17)
Figure 3.7: Boost converter equivalent circuits for DCM, (a) $S_1$ is on and $S_2$ is off, (b) $S_1$ is off and $S_2$ is on, (c) both switches are off.

From (3.15) the inductor and $S_2$ current is expressed as

\[
i_L(t) = i_{S2}(t) = \frac{1}{L} \int_{t}^{t+DT} v_L \, dt + i_L(DT) = \frac{1}{L} \int_{t}^{t+DT} (V_{IN} - V_{OUT}) \, dt + i_L(DT) = \frac{V_{IN} - V_{OUT}}{L} (t - DT) + \frac{V_{IN}DT}{L}.
\]
where $i_L(DT)$ is the maximum (peak) current at $t = DT$. The inductor current at the end of this phase $i_L((D + D_1)T)$ is equal to the minimum (initial) current $i_L(0) = 0$.

The peak-to-peak inductor current can be expressed as a function of $D_1$ in this phase as

$$
\Delta i_L = \frac{1}{L} \int_{(D+D_1)T}^{DT} v_L dt = \frac{1}{L} \int_{(D+D_1)T}^{DT} (V_{IN} - V_{OUT}) dt = \frac{(V_{OUT} - V_{IN}) D_1 T}{L} = \frac{(V_{OUT} - V_{IN}) D_1}{f_{SW} L}. \quad (3.19)
$$

This phase ends at $t = (D + D_1)T$, when $S_2$ is turned off, while $S_1$ is still off.
Phase 3

The third phase starts when switch $S_2$ opens while switch $S_1$ is left open. The voltage across $S_1$ is $V_{IN}$ and the voltage across $S_2$ is $V_{IN} - V_{OUT}$. The voltage across the inductor is zero. The currents through $S_1$, $S_2$, and the inductor are all zero. The current waveforms in all three phases are shown in Figs. 3.9 to 3.11.

Voltage gain

Using the volt-second balance and referring to Fig. 3.8,

$$V_{IN} DT = (V_{OUT} - V_{IN}) D_1 T,$$  \hspace{1cm} (3.20)
resulting in

$$M = \frac{V_{OUT}}{V_{IN}} = \frac{I_{IN}}{I_{OUT}} = 1 + \frac{D}{D_1}, \quad 1 < M < +\infty.$$  (3.21)

### 3.2 Structure of ideal step-down dc-dc converters

Fig. 3.12 shows the schematic of a step-down (buck) dc-dc converter, the output voltage $V_{OUT}$ is lower than the input voltage $V_{IN}$. The converter consists of an inductor $L$, two switches $S_1$ and $S_2$ controlled by phases $\Phi_1$ and $\Phi_2$, respectively, a filter capacitor $C$, and a load resistor $R$. Switches $S_1$ and $S_2$ are switched at a clock frequency $f_{SW} = 1/T$, with duty cycle $D$ defined as the time when $S_1$ is on divided by the time interval $T$. Similar to the boost converter, a buck dc-dc converter can operate in two conduction modes: the continuous conduction mode (CCM), and the discontinuous conduction mode (DCM). In CCM the current through the inductor $i_L(t)$ flows during the entire cycle. On the other hand, in DCM, $i_L(t)$ falls down to zero, remains at zero for some time, and then starts to increase.

#### 3.2.1 Continuous conduction mode

A buck converter in CCM works in two phases. The equivalent circuits of both phases are shown in Fig. 3.13. The first phase is bound by the time interval $0 < t \leq DT$, where $\phi_1$ is high and $\phi_2$ is low, resulting in $S_1$ being on and $S_2$ being off, respectively. The voltage across the inductor $v_L$ is equal to the $V_{IN} - V_{OUT}$; therefore, the inductor is charged by the voltage source causing the inductor current $i_L(t)$ to increase from its minimum value $I_{Lmin}$ to its maximum value $I_{Lmax}$ with
a slope of $(V_{IN} - V_{OUT})/L$. During this time interval, the energy is transferred from the dc supply to the inductor, capacitor, and load as shown in Fig. 3.13(a).

The second phase starts at time $t = DT$ and lasts until the end of the period $T$. In this phase, $\phi_1$ is low and $\phi_2$ is high, hence, $S_1$ is off and $S_2$ is on as shown in Fig. 3.13(b). Because the inductor current waveform is a continuous function of time, it flows in the same direction. The voltage across the inductor, $v_L$, becomes equal to $-V_{OUT}$. The inductor current $i_L(t)$ decreases from its maximum value $I_{L_{max}}$ to its minimum value $I_{L_{min}}$ with a slope of $-V_{OUT}/L$. During this interval the input source is disconnected from the circuit. The inductor and the capacitor form an energy reservoir to maintain the load voltage and current.

**Phase 1**

The first phase starts when switch $S_1$ closes and switch $S_2$ opens. The current through $S_2$ is zero and the voltage across it is $-V_{IN}$. The voltage across $S_1$ is zero. The linearized voltage across the inductor $L$ in phase 1 is shown in Fig. 3.14 and is given by
The inductor charges in this phase with a current $i_L(t)$ which is also equal to the current in $S_1$ in phase 1 and is expressed as

$$i_L(t) = i_{S1}(t) = \frac{1}{L} \int_0^t v_L dt + i_L(0) = \frac{V_{IN} - V_{OUT}}{L} t + i_L(0), \quad (3.23)$$

where $i_L(0)$ is the minimum (initial) current at $t = 0$. The maximum (peak) inductor current is given by

$$i_L(DT) = (V_{IN} - V_{OUT})\frac{DT}{L} + i_L(0). \quad (3.24)$$

The inductor current $i_L(t)$, $S_1$ current $i_{S1}(t)$, and $S_2$ current $i_{S2}(t)$ in phase 1 are shown in Figs. 3.15 to 3.17, respectively.

This phase ends at $t = DT$, when $S_1$ is turned off, and $S_2$ is turned on.

### Phase 2

The second phase starts when switch $S_1$ opens and switch $S_2$ closes. The current through $S_1$ is zero and the voltage across it is $V_{IN}$. The voltage across $S_2$ is zero. The linearized voltage across
Figure 3.15: The linearized current through the inductor, $i_L(t)$, in CCM.

Figure 3.16: The linearized current through $S_1$, $i_{S1}(t)$, in CCM.

Figure 3.17: The linearized current through $S_2$, $i_{S2}(t)$, in CCM.
the inductor $L$ in phase 2 is shown in Fig. 3.14 and is given by

$$ v_L(t) = -V_{OUT} = L \frac{di_L}{dt}, $$

(3.25)

The inductor discharges in this phase with a current $i_L(t)$, which is equal to the current in $S_2$ in phase 2 and is found to be

$$ i_L(t) = i_{S2}(t) = \frac{1}{L} \int_{DT}^{t} v_L \, dt + i_L(DT) = \frac{-V_{OUT}}{L} \int_{DT}^{t} \, dt + i_L(DT) = \frac{-V_{OUT}}{L} (t - DT) + i_L(DT), $$

(3.26)

where $i_L(DT)$ is the maximum (peak) current at $t = DT$. The inductor current at the end of this phase $i_L(T)$ is equal to the minimum (initial) current $i_L(0)$.

This phase ends at the end of the period when $t = T$ when $S_2$ is turned off and $S_1$ is turned on again.

**Voltage gain**

The average voltage value across the inductor in steady state using the volt-second balance is zero. Thus

$$ V_L = \frac{1}{T} \int_{0}^{T} v_L \, dt = 0. $$

(3.27)

From Fig. 3.14 this can be expressed as

$$ (V_{IN} - V_{OUT})DT = V_{OUT}(1 - D)T \Rightarrow V_{OUT} = DV_{IN}. $$

(3.28)

It follows that the ratio between the dc output voltage, $V_{OUT}$, and the dc input voltage, $V_{IN}$, for an ideal converter is

$$ M = \frac{V_{OUT}}{V_{IN}} = \frac{I_{IN}}{I_{OUT}} = D, $$

(3.29)

where $I_{IN}$ and $I_{OUT}$ are the average input and output currents, respectively. It should also be noted that for an ideal converter $0 < M < 1$. 
From (3.23), (3.24), and (3.28), the peak-to-peak value of the inductor current $\Delta i_L$ is then

$$\Delta i_L = i_L(DT) - i_L(0) = \frac{(V_{IN} - V_{OUT}) DT}{L} - \frac{(V_{IN} - V_{OUT}) D}{L f_{SW}} = \frac{V_{OUT} (1 - D)}{L f_{SW}}. \quad (3.30)$$

The peak switch current (for both $S_1$ and $S_2$) is given by

$$I_{S1max} = I_{S2max} = I_{OUT} + \frac{\Delta i_L}{2}. \quad (3.31)$$

### 3.2.2 Discontinuous conduction mode

A buck converter in DCM works in three phases. The equivalent circuits are shown in Fig. 3.18. The first phase starts at $t = 0$ and ends at $t = DT$, as shown in Fig. 3.18(a). During this phase, $\phi_1$ is high ($S_1$ is on) and $\phi_2$ is low ($S_2$ is off). The voltage across the inductor $v_L$ is equal to $V_{IN} - V_{OUT}$ and therefore, the inductor is charged by the voltage source causing the inductor current $i_L(t)$ to increase from its minimum value $I_{Lmin} = 0$ to its maximum value $I_{Lmax}$ with a slope of $V_{IN} - V_{OUT}/L$.

The second phase, shown in Fig. 3.18(b), starts at time $t = DT$ and ends at time $t = (D + D_1) T$, where $D_1$ is the time at which $S_2$ is on divided by the total period $T$. In this phase, $S_1$ is off and $S_2$ is on. The inductor starts acting as a current source and gets discharged into the filter capacitor and the load. The voltage across the inductor becomes equal to $-V_{OUT}$. The inductor current $i_L(t)$ decreases from its maximum value $I_{Lmax}$ to zero with a slope of $-V_{OUT}/L$.

The last phase starts at time $t = (D + D_1) T$ and ends at $t = T$. Both switches are off in this phase, thus the current through the inductor becomes zero, making the voltage across it equal to zero. The equivalent circuit is shown in Fig. 3.18(c).

**Phase 1**

During this time interval $S_1$ is on and $S_2$ is off, the voltage across $S_1$ is zero, the voltage across $S_2$ is $-V_{IN}$, and the voltage across the inductor is shown in Fig. 3.19 and is given by

$$v_L(t) = V_{IN} - V_{OUT} = L \frac{di_L}{dt}, \quad i_L(0) = 0. \quad (3.32)$$
The inductor current is equal to the $S_1$ current and is equal to
\[
i_L(t) = i_{S1}(t) = \frac{1}{L} \int_0^t v_L \, dt + i_L(0) = \frac{1}{L} \int_0^t (V_{IN} - V_{OUT}) \, dt + 0 = \frac{V_{IN} - V_{OUT}}{L} \cdot t. \tag{3.33}
\]
CHAPTER 3. THEORY OF OPERATION OF STEP-UP AND STEP-DOWN CONVERTERS

Figure 3.19: The linearized voltage across the inductor, \( v_L(t) \), in DCM.

The peak inductor current which is equal to \( \Delta i_L \) in DCM is given by

\[
i_L(DT) = \Delta i_L = \frac{(V_{IN} - V_{OUT}) DT}{L} = \frac{(V_{IN} - V_{OUT}) D}{L f_{SW}}. \tag{3.34}
\]

This phase ends when \( S_1 \) turns off and \( S_2 \) turns on.

**Phase 2**

The second phase starts when switch \( S_1 \) opens and switch \( S_2 \) closes. The current across \( S_1 \) is then zero and the voltage across it is \( V_{IN} \). The voltage across \( S_2 \) is zero. The linearized voltage across the inductor \( L \) in phase 2 is shown in Fig. 3.19 and is given by

\[
v_L(t) = -V_{OUT} = L \frac{di_L}{dt}. \tag{3.35}
\]

From (3.33) the inductor and \( S_2 \) current is expressed as

\[
i_L(t) = i_{S2}(t) = \frac{1}{L} \int_{DT}^{t} v_L dt + i_L(DT) = \frac{1}{L} \int_{DT}^{t} -V_{OUT} dt + i_L(DT)
\]

\[
= -\frac{V_{OUT}}{L} (t - DT) + i_L(DT) = -\frac{V_{OUT}}{L} (t - DT) + \frac{(V_{IN} - V_{OUT}) DT}{L}, \tag{3.36}
\]
where $i_L(DT)$ is the maximum (peak) current at $t = DT$. The inductor current at the end of this phase $i_L((D + D_1)T)$ is equal to the minimum (initial) current $i_L(0) = 0$.

The peak-to-peak inductor current can be expressed as a function of $D_1$ in this phase as

$$\Delta i_L = \frac{1}{L} \int_{(D + D_1)T}^{DT} v_L dt = \frac{1}{L} \int_{(D + D_1)T}^{DT} -V_{OUT} dt = \frac{V_{OUT} D_1 T}{L} = \frac{V_{OUT} D_1 f_{SW} L}{L}. \tag{3.37}$$

This phase ends at $t = (D + D_1)T$, when $S_2$ is turned off, while $S_1$ is still off.

**Phase 3**

The third phase starts when switch $S_2$ opens while switch $S_1$ is left open. The voltage across $S_1$ is $V_{IN} - V_{OUT}$ and the voltage across $S_2$ is $-V_{OUT}$. The voltage across the inductor is zero. The
currents through $S_1$, $S_2$, and the inductor are all zero. The current waveforms in all three phases are shown in Figs. 3.20 to 3.22.

**Voltage gain**

Using the volt-second balance and referring to Fig. 3.19,

$$(V_{IN} - V_{OUT}) DT = V_{OUT} D_1 T,$$  

resulting in

$$M = \frac{V_{OUT}}{V_{IN}} = \frac{I_{IN}}{I_{OUT}} = \frac{D}{D + D_1}, \quad 0 < M < 1.$$  

(3.39)

### 3.3 Summary

In this chapter, the basic models of both step-up and step-down dc-dc converters were introduced. The theory of operation for dc-dc converters in both conduction modes was presented. Based on these models, complete models of a fully integrated step-up and step-down dc-dc converters will be developed in the following chapters. These models will take all the relevant resistive and capacitive losses into consideration.
Chapter 4

Review of existing models of on-chip inductors

In CMOS circuits, interconnections account for more than half of the dynamic power dissipation and highly contribute to the delays, affecting the overall chip performance. While scaling generally improves the speed of transistors, RC delays of interconnection lines are usually more difficult to improve. With the half-pitch decreasing at any technology node, the interconnection capacitance per unit length drops, while the resistance per unit length increases [34]. Additionally, as the CMOS technology advances, the interconnection variability decreases and more accurate models become crucial for calculating delays and power dissipation. While interconnect capacitances have been studied extensively [35], less accurate approximations based on heuristic geometrical arguments are used for estimating the resistances.

Another significant reason for analyzing the resistance of metal segments is calculating the parasitic resistance of spiral inductors. Inductors are key elements in integrated circuits such as dc-dc converters and voltage controlled oscillators. The parasitic resistance of an inductor is an important design parameter, that sets a maximum bound to the allowable inductance based on area and frequency constraints. Finding an accurate value of the resistance requires calculating the current density distribution. The current density in a polygonal spiral inductor is different from that in a rectangular strip, since a spiral has bends which lead to high current density values around the inner corners and low current density values around the outer corners. Electromagnetic solvers fail to determine the current density around sharp inner corners fail due to non-convergence. Consequently, an analytical approach targeting the non-convergence problem and hence the resistance in corners is essential.

The lossy nature of passive devices is rooted in physical phenomena which convert electrical
energy into other, unrecoverable forms of energy. The quality factor of integrated passive devices depends on the material properties used in constructing the ICs. In particular, the semiconductor substrate and metal layers used to build the device play the most significant role [36,37].

The optimization of the process parameters for optimizing the inductor performance has been thoroughly studied [15,38]. Therefore, the focus of this chapter is to study the geometrical parameters for different inductor shapes and the way those parameters affect the values of inductance and parasitic resistance.

Inductors are constructed using a single or multiple metal layers, typically made of aluminium\(^1\). An inductor is wound using metal conductors of finite, limited conductivity. Most of the reactive energy is stored in the magnetic field of the inductor, but a portion of this energy is lost to heat in the volume of the inductor. The main losses which will be discussed are metal losses and substrate induced losses.

Metal losses are significant, even in the absence of the substrate effect, when the frequency increases the current distribution in the metal layers changes due to eddy currents. These in turn result in skin and proximity effects, current crowding, and current constriction. Currents tend to accumulate at the outer layer of conductors at higher frequencies, hence the effective width decreases. This in turn will increase the parasitic resistance, increasing the losses as will be seen in the following sections.

Since integrated inductors usually reside near a conductive Si substrate, as a consequence, the substrate becomes a source of loss and a frequency limitation. The Si resistivity varies from 10 k\(\Omega\)-cm to 0.001 \(\Omega\)-cm [39]. Some proposed solutions include removing the substrate from underneath the inductor by selective etching [40], and adding a patterned shield [41,42].

In Section 4.1, the inductor lumped electrical model is introduced. Different expressions for calculating the inductance are presented in Section 4.2. An expression for calculating the parasitic resistance, taking the frequency into consideration is also shown in Section 4.3.

4.1 Electrical lumped model

A planar spiral inductor can be seen as the series connection of a number of metal segments as shown in Fig. 4.1. the spiral inductors used here are Archimedean spirangles, which are similar to Archimedean spirals but they are made out of straight line segments, instead of curves. The total inductance is the sum of the self-inductances of the individual segments plus the mutual inductances between segments, which depend on the relative directions of the currents in each

\(^1\)Copper is currently also being used for the thicker top layer for its higher conductivity.
Figure 4.1: A square spiral inductor.
segment. Since the inductor will eventually be used in a larger circuit, it is preferable to model the spiral inductor with a low-order model of a planar spiral inductor as shown in Fig. 4.2. The model is accurate up until the resonant frequency, which suffices for integrated power converters, since the switching frequencies for dc-dc converters are well below 1 GHz (100 to 500 MHz) \[5\]. The model makes it easier to deal with the inductor as one lumped element with two ports. The model consists of: the inductance $L$, the frequency-dependent ohmic losses due to skin and proximity effects $R_L$, the combination of the crosstalk capacitance (parasitic capacitive coupling between adjacent metal segments) and the overlap capacitance (parasitic capacitive coupling between the spiral and the underpass) $C_L$, the oxide capacitance between the inductor and the substrate $C_{ox}$, the parasitic capacitive coupling into the substrate $C_{Si}$, and the ohmic loss in the conductive substrate $R_{Si}$.

By inserting a patterned ground shield with polysilicon slots orthogonal to the spiral, the inductor’s electric field is blocked from entering the silicon and hence substrate-coupling suppression is delivered \[37,42\]. Other advantages of the patterned ground shield include: making the inductor’s behaviour independent from variations in the substrate resistivity, and making the inductor behaviour easier to model. The simplified model of a planar spiral inductor with a patterned ground shield is shown in Fig. 4.3. As mentioned earlier, the shield helps to eliminate the
resistive and capacitive coupling to the substrate. Therefore, \( R_P \) is \( \infty \) and \( C_P \) is given by

\[
C_P = C_{ox} = \frac{w l_{tot} \varepsilon_{ox}}{2 t_{ox,po}},
\]

where \( l_{tot} \) is the total length of the spiral inductor, \( \varepsilon_{ox} = 3.453 \times 10^{-11} \) F/m is the oxide permittivity, and \( t_{ox,po} \) is the oxide thickness between the spiral and the polysilicon layer. For most practical inductors, it is sufficient to model \( C_L \) as the sum of all overlap capacitances, which is given by

\[
C_L = \frac{w^2 n \varepsilon_{ox}}{t_{ox,M-M}},
\]

where \( t_{ox,M-M} \) is the oxide thickness between the spiral and the underpass. The expressions for \( L \) and \( R_L \) are explained in detail in following sections.

### 4.2 Inductance

Planar spiral inductors can be defined by a combination of process, design, and geometrical parameters. The technology parameters include the resistivity \( \rho \), the thickness \( t \) of the metal layer, and the minimum allowable spacing between metal segments \( s_{min} \).

The design parameters are the total inductor area and the frequency of operation \( f \). The inductance is frequency-dependant, therefore, as the frequency changes, the current distribution in each metal segment also changes. When the effective cross-sectional area of the segments decreases at increasing frequencies, the current density increases, increasing the ac resistance...
(skin effect). The rate of increase is proportional to the effective depth of penetration $\delta$ of the current. In a multi-conductor element, the increase in resistance is attributed to both the skin effect and the effect of nearby conductors (proximity effects). In the case of an inductor, nearby conductors enhance the magnetic field causing the ac resistance to increase even further at increasing frequencies [39].

Finally, the main geometrical parameters are the shape (e.g. square, hexagonal, octagonal, circular), as shown in Fig. 4.4, the outer diameter $d_{\text{out}}$, the segment width $w$, the spacing between segments $s$, and the number of turns $n$. The parameters $w$, $s$, and $n$ are constrained by $d_{\text{out}}$ and each of them affects both values of inductance and series parasitic resistance in a different way.

The inductance of a spiral inductor can be calculated in multiple ways. The inductance can be calculated using lumped-element models with a good accuracy, however it leads to complex expressions. A numerical solution can also be acquired using three-dimensional finite-element simulators, and even though the results are very accurate they require long run times. Alternatively, different simple expressions were derived which predict the value of the inductance with typical errors in the range of 20% compared to the field solver simulations [43–45]. Three more accurate expressions for integrated inductors are commonly used: the modified Wheeler expression, the current sheet approximation, and the data fitting monomial expression [16].

### 4.2.1 Additional geometrical parameters

In addition to $w$, $s$, and $n$, supplementary geometrical parameters are defined. The inner diameter $d_{\text{in}}$ is the diameter of the hollow area inside the spiral. The average diameter is given by

$$d_{\text{avg}} = \frac{d_{\text{out}} + d_{\text{in}}}{2} = d_{\text{out}} - n w - (n - 1) s.$$  \hspace{1cm} \text{(4.3)}

The fill ratio $\rho_f$ indicates how hollow ($\rho_f$ is small when $d_{\text{out}} \approx d_{\text{in}}$) or full ($\rho_f$ is large when $d_{\text{out}} \gg d_{\text{in}}$) the spiral inductor is and is given by

$$\rho_f = \frac{d_{\text{out}} - d_{\text{in}}}{d_{\text{out}} + d_{\text{in}}} = \frac{n w + n s - s}{d_{\text{out}} - n w - n s + s}.$$  \hspace{1cm} \text{(4.4)}

### 4.2.2 Current sheet approximation expression

This expression is obtained by approximating the sides of the spirals by symmetrical current sheets of equivalent current densities [16]. For example, in a square inductor there are four
Figure 4.4: Polygonal inductors: (a) square, (b) hexagonal, (c) octagonal, (d) circular.
current sheets. The current sheets on adjacent sides are orthogonal to one another, while the opposite ones are parallel. The computation of the inductance is done by evaluating the self-inductance of a given sheet and the mutual inductance between opposite sheets. These self and mutual inductances are calculated using the concepts of geometric mean distance, arithmetic mean distance, and arithmetic mean square distance. The resulting expression is

\[
L_{gmd} = \frac{\mu d_{avg} c_1}{2} \left( \ln \frac{c_2}{\rho_f} + c_3 \rho_f + c_4 \rho_f^2 \right),
\]

where \(\mu\) is the relative magnetic permeability and coefficients \(c_1, c_2, c_3,\) and \(c_4\) are layout dependent as reported in Table 4.1 [16].

Table 4.1: Coefficients for current sheet approximation expression

<table>
<thead>
<tr>
<th>Shape</th>
<th>(c_1)</th>
<th>(c_2)</th>
<th>(c_3)</th>
<th>(c_4)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Square</td>
<td>1.27</td>
<td>2.07</td>
<td>0.18</td>
<td>0.13</td>
</tr>
<tr>
<td>Hexagonal</td>
<td>1.09</td>
<td>2.23</td>
<td>0.00</td>
<td>0.17</td>
</tr>
<tr>
<td>Octagonal</td>
<td>1.07</td>
<td>2.29</td>
<td>0.00</td>
<td>0.19</td>
</tr>
</tbody>
</table>

4.2.3 Data fitted monomial expression

This expression is based on a data fitting technique using a least-squares fit, with a library of 19000 inductors. The resulting expression is

\[
L_{mon} = \beta d_{out}^{\alpha_1} d_{avg}^{\alpha_2} \mu^{\alpha_3} s^{\alpha_4} n^{\alpha_5},
\]

where the coefficients \(\beta, \alpha_1, \alpha_2, \alpha_3, \alpha_4,\) and \(\alpha_5\) are layout dependent and given in Table 4.2.

Table 4.2: Coefficients for data fitted monomial expression

<table>
<thead>
<tr>
<th>Shape</th>
<th>(\beta)</th>
<th>(\alpha_1)</th>
<th>(\alpha_2)</th>
<th>(\alpha_3)</th>
<th>(\alpha_4)</th>
<th>(\alpha_5)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Square</td>
<td>1.62 \times 10^{-3}</td>
<td>-1.21</td>
<td>-0.147</td>
<td>2.4</td>
<td>1.78</td>
<td>-0.030</td>
</tr>
<tr>
<td>Hexagonal</td>
<td>1.28 \times 10^{-3}</td>
<td>-1.24</td>
<td>-0.174</td>
<td>2.47</td>
<td>1.77</td>
<td>-0.049</td>
</tr>
<tr>
<td>Octagonal</td>
<td>1.33 \times 10^{-3}</td>
<td>-1.21</td>
<td>-0.163</td>
<td>2.43</td>
<td>1.75</td>
<td>-0.049</td>
</tr>
</tbody>
</table>
4.2.4 Modified Wheeler expression

This expression is based on a simple modification to the Wheeler formula [46] that was originally developed for discrete inductors. The modified Wheeler formula for a polygonal spiral inductor is given by

\[
L_{mw} = \mu_1 \mu_0 \frac{n^2 d_{avg}}{1 + \mu_2 \rho_f}
\]

where \(\mu_0\) is the magnetic permeability of free space and \(\mu_1\) and \(\mu_2\) are shape-dependent coefficients shown in Table 4.3 [16].

Table 4.3: Coefficients for modified Wheeler expression

<table>
<thead>
<tr>
<th>Shape</th>
<th>(\mu_1)</th>
<th>(\mu_2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Square</td>
<td>2.34</td>
<td>2.75</td>
</tr>
<tr>
<td>Hexagonal</td>
<td>2.33</td>
<td>3.82</td>
</tr>
<tr>
<td>Octagonal</td>
<td>2.25</td>
<td>3.55</td>
</tr>
</tbody>
</table>

This work uses the modified Wheeler expression. The software tool ASITIC [47] was used for simulations, ASITIC is CAD tool that aids the circuit designer to optimize and model spiral inductors, transformers, capacitors, and substrate coupling. ASITIC calculations include the electrically induced losses and coupling as well as the magnetically induced eddy current losses. Skin effect and proximity effects, or eddy currents in the metallization, are also included [39]. The results from this analytical expression match the ASITIC simulator with errors typically in the range of 1 to 3%.

4.3 Series parasitic resistance

The parasitic series resistance of the inductor is one of the main components that determine the quality factor of an inductor. The resistance changes significantly as a function of frequency. For the frequency range of interest, the ac resistance follows a \(\sqrt{f}\) dependence as predicted by the
skin effect theory. Note that for higher frequency ranges, the ac resistance increases faster than $\sqrt{f}$ [36, 39]. The skin depth $\delta$ is approximated as

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_0 \mu_r}}, \quad (4.8)$$

where $\rho$ is the electrical resistivity of the material, $\mu_0$ is the magnetic permeability of free space, and $\mu_r$ is the relative permeability. An expression of the resistance including the skin depth of a conductor with finite thickness, is given by [17]

$$R = \frac{\rho}{\delta (1 - e^{-t/\delta})} \frac{l_{tot}}{w} = R^\square \frac{l_{tot}}{w}, \quad (4.9)$$

where $t$ is the metal layer thickness, $l_{tot}$ is the total inductor length, and $R^\square$ is a technology-dependent coefficient which is basically the sheet resistance taking the frequency and hence the skin depth into consideration. The resistance is a function of $l_{tot}/w$, which is the total number of squares of side $w$ included in the strip. Therefore, in order to accurately determine the resistance value, the total number of squares has to be accurately calculated. For example, in a rectangular strip of metal, calculating the number of squares is performed by dividing the total length of the strip over the width as shown in Fig. 4.5.

### 4.4 Summary

In this chapter, a detailed electrical lumped model was introduced in the first section. Three different models for calculating the inductance were discussed in the second section. The modified Wheeler expression was chosen for this work. The third section models the resistance of integrated inductors, taking the frequency into consideration.
Chapter 5

Modelling of integrated dc-dc converters

Fully integrated dc-dc converters have low values of inductance (nH) and capacitance (pF) [6, 9, 10]. These values are significantly lower than their off-chip counterparts. Therefore, to utilize smaller passive elements, fully-integrated converters usually operate at much higher switching frequencies (hundreds of MHz) [12, 31, 48–50]. High switching frequencies introduce switching losses, resulting in the models introduced in Chapter 2 not being sufficient to describe fully-integrated converters. A more accurate model, that takes different kinds of losses into consideration, is therefore crucial for fully modelling the system and finding important trade-offs.

In Section 5.1, mathematical steady-state models for both a boost and a buck converters which take all resistive losses into account are introduced. The non-idealities of the different components of a converter are modelled in Section 5.2 in order to also include all the capacitive losses. A complete efficiency model is then derived in Section 5.3.

5.1 A second-order mathematical model

Having multiple variables to consider, such as: the inductance value, the filter capacitance value, switching frequency, input voltage, MOSFET sizes, and duty cycle, combined with various requirements such as: output power, conversion efficiency, and output voltage ripple, results in the design process being very complex with multiple trade-offs to deal with. Since the scope of this work is fully-integrated converters, the design process becomes even more challenging, since the converters have to work at the limits of the IC technology they are implemented in [5, 51].

Similar to the model introduced in Section 3.1, various mathematical steady-state models based on small-ripple approximation have been introduced [52, 53]. These models can be used
with a fair accuracy when dealing with external passives and switches with relatively large values and low switching frequency in the kHz range. More recent models [21, 54] provide some extensions on the original models to accommodate further losses, however, they lack accuracy for monolithic converters. The mathematical model presented in this section is based on the differential equations for the boost converter, taking all the resistive losses into consideration [5, 13, 55–57].

5.1.1 Differential equations: boost converter

A general equivalent circuit for a practical boost converter that includes all major resistive losses is shown in Fig. 5.1. The input voltage source which can be the output of a battery, another converter, or a Universal Serial Bus (USB), is modelled as an ideal voltage source $V_{IN}$ with a resistance $R_{IN}$ in series. The inductor is modelled as an inductance $L$ with a series resistance $R_L$. The capacitor is modelled as a capacitance $C$ with a series resistance $R_C$. Switches $S_1$ and $S_2$ are replaced with MOSFETs $M_1$ and $M_2$, respectively. In Fig. 5.2 the NMOS $M_1$ is modelled as a switch with a series on resistance between the drain and source $r_{DSn}$. Similarly, the PMOS $M_2$ is modelled as a switch with on resistance $r_{DSp}$.

\[1\text{Intrinsic MOSFET capacitances are ignored in this section.}\]
Figure 5.2: Boost converter equivalent circuit with the MOSFETs modelled as switches with a series on resistance.

Charging the inductor

The equivalent circuit for the charging of the inductor is shown in Fig. 5.3. For simplifying the notation, the circuit in Fig. 5.3(b) is used, where

\[ R_{EQ1} = R_L + R_{in} + r_{DSn}. \] (5.1)

The initial inductor current in this phase, which is also the value of \( i_L(t) \) at the end of the preceding discharge phase, is defined as

\[ i_L(0) = I_{L\text{min}}. \] (5.2)

From the discussion in Chapter 2, \( I_{L\text{min}} \) is zero in DCM, and has a positive value in CCM.

\[
\begin{cases}
    I_{L\text{min}} = 0 & \leftarrow \text{DCM} \\
    I_{L\text{min}} > 0 & \leftarrow \text{CCM}
\end{cases}
\] (5.3)

The differential equation of the circuit in this phase is then given by

\[ L \frac{di_L(t)}{dt} + R_{EQ1} i_L(t) - V_{IN} = 0. \] (5.4)
Figure 5.3: Schematic diagrams for the charge phase: (a) equivalent circuit. (b) simplified equivalent circuit.

Solving (5.4) to find \( i_L(t) \) using the initial condition (5.2) leads to

\[
i_L(t) = \frac{V_{IN}}{R_{EQ1}} + \left( I_{L_{\text{min}}} - \frac{V_{IN}}{R_{EQ1}} \right) e^{-t \frac{R_{EQ1}}{L}}.
\] (5.5)

**Discharging the inductor**

Similarly to the previous phase, in the discharge phase, the simplified equivalent circuit is shown in Fig. 5.4(b), where \( R_{EQ2} \) is given by

\[
R_{EQ2} = R_L + R_{IN} + r_{DSp}.
\] (5.6)

The initial inductor current in this phase, which is also the value of \( i_L(t) \) at the end of the charge phase, is defined as

\[
i_L(0) = I_{L_{\text{max}}}.
\] (5.7)

The circuit differential equation for the discharge phase is given by

\[
\frac{d^2i_L(t)}{dt^2} \left( \frac{R_C L}{R} + L \right) + \frac{di_L(t)}{dt} \left( \frac{L}{R_C} + \frac{R_C (R + R_{EQ2})}{R} + R_{EQ2} \right) + i_L(t) \frac{(R + R_{EQ2})}{R_C} - \frac{V_{IN}}{R_C} = 0.
\] (5.8)

The second order differential equation can be solved given two initial conditions, one is from (5.7), and the other is given by
Figure 5.4: Schematic diagrams for the discharge phase: (a) equivalent circuit, (b) simplified circuit.

\[
\frac{di_L(0)}{dt} = I_{L_{\text{max}}} \frac{R^2 - (R + R_C)(R + R_{EQ2})}{L(R + R_C)} - V_{C_{\text{min}}} \frac{R}{L(R + R_C)} + \frac{V_{IN}}{L}. \tag{5.9}
\]

Solving the second-order differential equation to find \(i_L(t)\) leads to

\[
i_L(t) = I_S + A_1 e^{s_1 t} + A_2 e^{s_2 t}, \tag{5.10}
\]

where \(I_S\) is the steady state current given by

\[
I_S = \frac{V_{IN}}{R + R_{EQ2}}, \tag{5.11}
\]

and \(s_1\) and \(s_2\) are given by

\[
s_1 = -\frac{1}{2}(a + b), \quad s_2 = -\frac{1}{2}(a - b), \tag{5.12}
\]
with
\[
a = \frac{C RR_{EQ2} + C R C_{EQ2} + C RR + L}{C LR + C L R}
\] (5.13)
and
\[
b = \sqrt{\frac{(C (R_C + R) R_{EQ2} + C RR + L)^2 - 4C L (R_C + R) (R_{EQ2} + R)}{C^2 L^2 (R_C + R)^2}}.
\] (5.14)

The constants \(A_1\) and \(A_2\) are given by
\[
A_1 = (I_{L\max} (R + R_{EQ2}) (L (bC (R + R_C) - 1) + C (R (R_C + R_{EQ2}) + R C R_{EQ2}))) + V_{IN} (L (1 - bC (R + R_C)) - C (R (2R + R_C + R_{EQ2}) + R C R_{EQ2})) + 2C R V_{Cmin} (R + R_{EQ2}))/ (2b C L (R + R_C) (R + R_{EQ2})),
\] (5.15)
\[
A_2 = (I_{L\max} (R + R_{EQ2}) (L (bC (R + R_C) + 1) - C (R (R_C + R_{EQ2}) + R C R_{EQ2}))) + V_{IN} (L (-1 - bC (R + R_C)) + C (R (2R + R_C + R_{EQ2}) + R C R_{EQ2})) - 2C R V_{Cmin} (R + R_{EQ2}))/ (2b C L (R + R_C) (R + R_{EQ2})),
\] (5.16)

where \(V_{Cmin}\) is the minimum capacitor voltage at the end of the preceding charge phase.

### 5.1.2 Average output voltage: boost converter

After solving the differential equations of both phases, the average output voltage of the converter for both conduction modes can be calculated. In the following DCM analysis \(t_{ch}\) is defined as the time when the NMOS is conducting and the inductor is charging, \(t_{dis}\) is the time when the PMOS is conducting and the inductor is discharging, and \(t_d\) is defined as the time when both MOSFETs are off. The time interval that encloses both time intervals \(t_{dis}\) and \(t_d\) is referred to as \(t_{off}\). In CCM \(t_d\) is equal to zero and hence \(t_{off}\) is equal to \(t_{dis}\).

**DCM**

The maximum inductor current \(I_{L\max}\) in DCM is given by (5.5), which can also be written as
\[
I_{L\max} = \frac{V_{IN}}{R_{EQ1}} \left(1 - e^{-t_{ch} \frac{R_{EQ1}}{L}}\right),
\] (5.17)
in this equation $t$ is replaced with $t_{ch}$ and $I_{L_{min}}$ with zero. From (5.17) $I_{L_{max}}$ is a function of the input parameters $V_{IN}$ and $t_{ch}$. The current in the NMOS $i_{NMOS}(t)$ is equal to $i_{L}(t)$ in the charge phase, and is equal to zero otherwise. The current in the PMOS, $i_{PMOS}(t)$ is equal to $i_{L}(t)$ when the PMOS is on and the inductor is discharging which is given by (5.10). $i_{PMOS}(t)$ becomes zero some time into $t_{off}$ which can be calculated by equating (5.10) to zero for $t = t_{dis}$, making $i_{PMOS}(t)$ a function of both input and output parameters. In the discharge phase, $i_{L}(t)$ branches into $i_{C}(t)$ through the filter capacitor and $i_{R}(t)$ through the load resistor. Since steady state analysis is the main concern here, the dc component of the current will flow only through the resistor and the ac component will flow through the capacitor (i.e. $i_{R}(t) = i_{PMOS}(t)$) [5]. The average output voltage can then be calculated using

$$V_{OUT} = RI_{PMOS} = R \frac{1}{T} \int_{0}^{T} i_{PMOS}(t) \, dt \simeq R \frac{I_{L_{max}}}{2} \frac{t_{dis}}{T}, \quad (5.18)$$

It is to be noted that $t_{dis}$ is required to calculate $V_{OUT}$ which can be calculated using (5.10) which would in turn, require calculating $V_{C_{min}}$. $C$ is discharged through $R$ resulting in an exponential RC discharge waveform which can be expressed as

$$V_{C_{min}} \simeq V_{OUT} e^{-\frac{t_{ch} + t_{dis}}{2RC}} = V_{OUT} e^{-\frac{T - t_{dis}}{2RC}}. \quad (5.19)$$

The next step is calculating $V_{C_{max}}$ in order to find the output ripple voltage $\Delta V_{OUT}$. In a similar fashion the capacitor is charging and the voltage across it is given by

$$V_{C_{max}} = V_{C_{min}} e^{\frac{t_{ch} + t_{dis}}{RC}} = V_{C_{min}} e^{\frac{T - t_{dis}}{RC}}. \quad (5.20)$$

In deriving (5.19) and (5.20) it was assumed that there is no effect of $R_{C}$ on the average $v_{C}(t)$, $V_{C}$, which is due to the fact that in steady state the voltage across $R_{C}$ will have equal positive and negative parts cancelling out the effect of $R_{C}$ on $V_{C}$. This however, is not that case for calculating $\Delta V_{OUT}$, since a larger $R_{C}$ leads to a larger voltage drop across it, and hence a larger value of $\Delta V_{OUT}$. $\Delta V_{OUT}$ is then given by

$$\Delta V_{OUT} = (V_{C_{max}} + (I_{L_{max}} - I_{R})R_{C}) - (V_{C_{min}} - I_{R}R_{C}). \quad (5.21)$$
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CCM

The main difference between CCM and DCM is that \( I_{L_{\text{min}}} \) is a finite, positive value, and that \( t_d \) is zero. The maximum inductor current \( I_{L_{\text{max}}} \) can now be written in CCM as

\[
I_{L_{\text{max}}} = \frac{V_{IN}}{R_{EQ1}} + \left( I_{L_{\text{min}}} - \frac{V_{IN}}{R_{EQ1}} \right) e^{-\frac{t_{\text{on}}}{L R_{EQ1}}}. \tag{5.22}
\]

The average output voltage in CCM can be calculated similarly to DCM by averaging the current in the PMOS, \( i_{PMOS}(t) \)

\[
V_{OUT} = I_{PMOS} R = R \frac{1}{T} \int_0^T i_{PMOS}(t) \, dt \simeq R \frac{I_{L_{\text{min}}} + I_{L_{\text{max}}}}{2} \frac{t_{\text{off}}}{T}. \tag{5.23}
\]

During \( t_{\text{ch}} \), \( C \) is discharged through \( R \), and \( V_{C_{\text{min}}} \) is given by

\[
V_{C_{\text{min}}} \simeq V_{OUT} e^{-\frac{t_{\text{ch}}}{RC}}. \tag{5.24}
\]

Similarly, \( V_{C_{\text{max}}} \) is given by

\[
V_{C_{\text{max}}} = V_{C_{\text{min}}} e^{\frac{t_{\text{ch}}}{RC}}. \tag{5.25}
\]

\( \Delta V_{OUT} \) can be calculated using the DCM expression in (5.21).

5.1.3 Differential equations: buck converter

The equivalent circuit for a buck converter that includes all major resistive losses is shown in Fig. 5.5. The input voltage source is modelled as an ideal voltage source \( V_{IN} \) with a resistance \( R_{IN} \) in series. The inductor is modelled as an inductance \( L \) with a series resistance \( R_L \). The capacitor is modelled as a capacitance \( C \) with a series resistance \( R_C \). Switches \( S_1 \) and \( S_2 \) are replaced with MOSFETs \( M_1 \) and \( M_2 \), respectively. In Fig. 5.6 the PMOS \( M_1 \) is modelled as a switch with a series on resistance between the drain and source \( r_{DSP} \). Similarly, the NMOS \( M_2 \) is modelled as a switch with on resistance \( r_{DSn} \).

Charging the inductor

The equivalent circuit for the charging of the inductor \( L \) is shown in Fig. 5.7 where

\[
R_{EQ1} = R_L + R_{\text{in}} + r_{DSP}. \tag{5.26}
\]
Figure 5.5: Buck converter equivalent circuit with parasitic elements.

Figure 5.6: Buck converter equivalent circuit with the MOSFETs modelled as switches with a series on resistance.
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Figure 5.7: The equivalent circuit for the charge phase.

The initial inductor current in this phase, which is also the value of \( i_L(t) \) at the end of the preceding discharge phase, is defined as

\[
i_L(0) = I_{L_{min}}, \tag{5.27}
\]

where \( I_{L_{min}} \) is zero in DCM, and it has a positive value in CCM.

The differential equation of the circuit in this phase is second-order and is given by

\[
\frac{d^2 i_L(t)}{dt^2} \left( \frac{R_L}{R} + L \right) + \frac{di_L(t)}{dt} \left( \frac{L}{RC} + \frac{R_C(R+R_{EQ1})}{R} + R_{EQ1} \right) + i_L(t) \frac{(R+R_{EQ1})}{RC} - \frac{V_{IN}}{RC} = 0, \tag{5.28}
\]

where the two initial conditions to solve this equation are given by (5.27) and

\[
\frac{di_L(0)}{dt} = I_{L_{min}} \left( R - \frac{(R_{EQ1} + R)(R + R_C)}{R} \right) \frac{R}{L(R + R_C)} + \frac{V_{IN}}{L} - \frac{V_{OUT}}{L(R + R_C)}. \tag{5.29}
\]

In (5.29) the initial voltage across \( C \) is approximated as \( V_{OUT} \), which is valid for both conduction modes.

**Discharging the inductor**

Similar to the previous phase, in the discharge phase, the equivalent circuit is shown in Fig. 5.8, where \( R_{EQ2} \) is given by

\[
R_{EQ2} = R_L + r_{DSn}. \tag{5.30}
\]

The initial inductor current in this phase, which is also the value of \( i_L(t) \) at the end of the charge phase, is defined as

\[
i_L(0) = I_{L_{max}}. \tag{5.31}
\]
Figure 5.8: The equivalent circuit for the discharge phase.

The differential equation of the discharge phase is given by

\[
\frac{d^2 i_L(t)}{dt^2} \left( \frac{R_C L}{R} + L \right) + \frac{di_L(t)}{dt} \left( \frac{L}{R C} + \frac{R_C (R + R_{EQ2})}{R} + R_{EQ2} \right) + i_L(t) \frac{(R + R_{EQ2})}{RC} = 0. \tag{5.32}
\]

The second order differential equation can be solved given two initial conditions, one is from (5.31), and the other is given by

\[
\frac{di_L(0)}{dt} = I_{L_{\text{max}}} \left( R - \frac{(R_{EQ2} + R)(R + R_C)}{R} \right) \frac{R}{L(R + R_C)} - V_{OUT} \frac{R}{L(R + R_C)}. \tag{5.33}
\]

### 5.1.4 Average output voltage: buck converter

For the output voltage calculation, we use the time-domain solutions to both differential equations (5.28) and (5.32). This method is similar to the one developed for the boost converter. In the following DCM analysis, \(t_{ch}\) is defined as the time when the PMOS is conducting and the inductor is charging, \(t_{dis}\) is the time when the NMOS is conducting and the inductor is discharging, and \(t_d\) is defined as the time when both MOSFETs are off. The time interval that encloses both time intervals \(t_{dis}\) and \(t_d\) is referred to as \(t_{\text{off}}\). In CCM, \(t_d\) is equal to zero and hence \(t_{\text{off}}\) is equal to \(t_{\text{dis}}\).

#### DCM

The maximum inductor current \(I_{L_{\text{max}}}\) in DCM is determined by the solution of (5.28), which is valid for the charge phase for \(i_L(t) = I_{L_{\text{min}}} = 0\) and \(t = t_{ch}\). Therefore, \(I_{L_{\text{max}}}\) is a function of the input parameters \(V_{IN}, V_{OUT},\) and \(t_{ch}\). Similarly to calculate \(i_L(t)\) during the discharge phase, the solution of (5.32) is used, and \(I_{L_{\text{min}}}\) becomes zero at \(t = t_{\text{dis}}\). Therefore, \(I_{L_{\text{min}}}\) is a function of the input parameters \(V_{OUT}, I_{L_{\text{max}}},\) and \(t_{\text{dis}}\).
Similar to the boost converter, $i_L(t)$ is divided into $i_C(t)$ through the filter capacitor and $i_R(t)$ through the load resistor. Since the steady state current through the capacitor is zero, $i_L(t)$ flows entirely in $R$. Therefore, $V_{OUT}$ is given by

$$V_{OUT} = R I_L = R \frac{1}{T} \int_0^T i_L(t) \, dt \simeq R_{EQ} \frac{I_{Lmax} t_{ch} + t_{dis}}{T}, \quad (5.34)$$

The calculation method of $\Delta V_{OUT}$ is based on the calculation of the injected positive charge change into the filter capacitor $C$. Therefore, $i_C(t)$ is calculated using

$$i_C(t) = i_L(t) - i_R(t) \simeq i_L(t) - \frac{V_{OUT}}{R}, \quad (5.35)$$

where $i_L(t)$ is calculated by the time-domain solution of (5.28) for the charge phase, yielding $i_{C_{charge}}(t)$. For the discharge phase $i_L(t)$ is calculated by the time-domain solution of (5.32), yielding $i_{C_{discharge}}(t)$. $\Delta Q$ is then calculated by integrating $i_{C_{charge}}(t)$ with respect to time from the time where it intersects the x-axis to $t_{ch}$ and $i_{C_{discharge}}(t)$ with respect to time from time zero to the time where it intersects the x-axis. The approximated maximum output voltage taking the voltage ripple into account is given by

$$V_{OUTmax} \simeq V_{OUT} + \frac{\Delta Q}{2C} - R_C \frac{I_{Lmax} - I_{OUT}}{2} = V_{Cmax} - R_C \frac{I_{Lmax} - I_{OUT}}{2}. \quad (5.36)$$

Similarly, the approximated minimum output voltage is

$$V_{OUTmin} \simeq V_{OUT} - \frac{\Delta Q}{2C} - R_C \frac{I_{Lmax} - I_{OUT}}{2} = V_{Cmin} - R_C \frac{I_{Lmax} - I_{OUT}}{2}. \quad (5.37)$$

From (5.36) and (Eqn:voutmin), $\Delta V_{OUT}$ can be expressed as

$$\Delta V_{OUT} \simeq V_{OUTmax} - V_{OUTmin} = \frac{\Delta Q}{C} + R_C (I_{Lmax} - I_{OUT}). \quad (5.38)$$

**CCM**

The main difference between CCM and DCM is that $I_{Lmin}$ is a positive value, and that $t_{d}$ is zero. During the charge phase in steady-state, $I_{Lmax}$ is determined by the time-domain solution of (5.28), for $t = t_{ch}$, which makes $I_{Lmax}$ a function of $V_{IN}$, $V_{OUT}$, $I_{Lmin}$, and $t_{ch}$. Similarly for the discharge phase $I_{Lmin}$ is found by solving (5.32) for $t = t_{dis}$, yielding $I_{Lmin}$ a function of $V_{OUT}$.
\( I_{L,\text{max}} \) and \( t_{\text{dis}} \). In steady-state, the charge balance of \( C \) again is zero, and the dc component of \( i_L(t) \) will only flow through the load resistance \( R \). The approximated equation of \( V_{\text{OUT}} \) is therefore given by

\[
V_{\text{OUT}} = I_L R = R \frac{1}{T} \int_0^T i_L(t) \, dt \simeq R \frac{I_{L,\text{min}} + I_{L,\text{max}}}{2}.
\]

(5.39)

\( \Delta V_{\text{OUT}} \) can be calculated using the DCM expression in (5.38).

### 5.2 Components non-idealities

In this section, the dynamic losses (i.e. switching losses) are introduced. The converter components are modelled, taking all parasitic capacitances into consideration. Those capacitances in addition to the above-mentioned resistances will contribute to power losses, which will in turn affect the output voltage ripple and the overall conversion efficiency. The power losses associated with each component are calculated in this section in order to provide a method for determining the dominant power losses.

#### 5.2.1 Inductor

A planar spiral inductor is constructed by a series connection of a number of metal segments. The total inductance is calculated by summing all the self-inductances of the individual segments and the mutual inductances between segments, which depend on the relative directions of the currents in each segment. Traditionally, discrete inductors were modelled using simple expressions [46, 58]. Integrated metal-track inductors have been modelled with more complex expressions [15, 16, 43–45] or lumped circuit components [36, 37, 42, 59–63]. More complex, frequency-independent models were proposed in [64–68].

Electrical wires have a self-inductance, that is proportional to their length and inversely proportional to their radius. For a straight segment with length \( l \), a circular cross section with radius \( r \), and a dielectric with a relative permeability \( \mu_r = 1 \), the inductance \( L \) is given by [58]

\[
L = \frac{l}{5} \left( \ln \left( \frac{2l}{r} \right) - \frac{3}{4} + \frac{r}{l} \right),
\]

(5.40)

where \( l \) and \( r \) are in mm and \( L \) is in nH.

The series parasitic resistance \( R_L \) is the main power loss factor in inductors. \( R_L \) is determined by the conductor length \( l \), the cross-sectional area \( A \), and the electrical resistivity \( \rho \). For a circular
cross-section, $R_L$ is given by

$$R_L = \frac{\rho l}{A} = \frac{\rho l}{\pi r^2}. \tag{5.41}$$

Since the current through the conductor is not constant, it should be noted that the series resistance is a function of the frequency. As the frequency increases, the current tends to flow in the outer layer of the conductor, decreasing the effective cross-sectional area, this in turn makes the series parasitic resistance larger and increases the power losses.

The resulting power loss is determined by [5]

$$P_{RL} = I_{L,RMS}^2 R_L = (I_{M1,RMS}^2 + I_{M2,RMS}^2) R_L, \tag{5.42}$$

where $I_{M1,RMS}$ and $I_{M2,RMS}$ are the root-mean-square currents through $M_1$ and $M_2$, respectively, for a boost or a buck converter. For DCM in both buck and boost converters these expressions are given by

$$I_{M1,RMS} = \sqrt{\frac{1}{T} \int_0^T i_{M1}^2(t) \, dt} \simeq I_{L_{max}} \sqrt{\frac{i_{ch}}{3T}}, \tag{5.43}$$

$$I_{M2,RMS} = \sqrt{\frac{1}{T} \int_0^T i_{M2}^2(t) \, dt} \simeq I_{L_{max}} \sqrt{\frac{i_{dis}}{3T}}. \tag{5.44}$$

For CCM these expressions are given by

$$I_{M1,RMS} = \sqrt{\frac{1}{T} \int_0^T i_{M1}^2(t) \, dt} \simeq \frac{i_{ch}}{T} \left( i_{L_{min}}^2 + I_{L_{min}}(I_{L_{max}} - I_{L_{min}}) + \frac{(I_{L_{max}} - I_{L_{min}})^2}{3} \right), \tag{5.45}$$

$$I_{M2,RMS} = \sqrt{\frac{1}{T} \int_0^T i_{M2}^2(t) \, dt} \simeq \frac{i_{off}}{T} \left( i_{L_{min}}^2 + I_{L_{min}}(I_{L_{max}} - I_{L_{min}}) + \frac{(I_{L_{max}} - I_{L_{min}})^2}{3} \right). \tag{5.46}$$

Integrated inductors, on the other hand, introduce their own parallel parasitic resistances, parasitic resistances due to the ohmic loss in the conductive substrate, parasitic substrate capacitances, and overlap capacitances. Therefore, a detailed discussion on modelling integrated inductors is provided in Chapter 4.
5.2.2 Capacitor

An integrated capacitor can be modelled as shown in Fig. 5.9. The equivalent circuit takes into consideration the parasitic series resistance $R_C$ which is the main loss factor, the parasitic series inductance $L_C$, and the parasitic parallel resistance $R_{Cp}$. In the full model of the dc-dc converter, the parasitic inductance is assumed to be small enough to be neglected and the parallel resistance is considered as part of the load resistance.

The parasitic series resistance is highly dependent on the geometry and layout of the integrated capacitor. $R_C$ has two main drawbacks on the converter: it increases the power loss and the ripple voltage. The power loss for a boost converter can be expressed as

$$P_{RC} = I_{M2,RMS}^2 R_C,$$

and for a buck converter as

$$P_{RC} = (I_{M2,RMS}^2 + I_{M2,RMS}^2) R_C.$$

Steep transients between the charge and discharge phases occur due to $R_C$, increasing the amplitude of $\Delta V_{OUT}$. Those transients are due to the fact that the current in the filter capacitor is discontinuous. Correspondingly, the odd harmonics have a significantly larger amplitude. This introduces a problem for the load circuitry and neighbouring circuits in terms of EMI.

Monolithic capacitors tend to introduce a leakage current, which can be modelled by the parasitic parallel resistor $R_{Cp}$. This leakage current is proportional to the size of the capacitor and the capacitance. The power loss introduced by this resistor is given by

$$P_{RCp} = \frac{V_{OUT,RMS}^2}{R_{Cp}}.$$

It should be taken into account that both parasitic resistances will depend on the implementation of the capacitor. On-chip capacitors are categorized into native and non-native [5]. The two
most used native types are the Metal-Oxide-Metal (MOM) and the Metal-Oxide-Silicon (MOS) capacitors. MOM capacitors are most suitable for deep-submicron technologies where the number of metal layers is high. MOM capacitors can withstand higher voltages than the nominal supply voltage and have relatively low parasitic resistance, however, their typical capacitive densities are relatively low ranging from 0.1 to 1.5 nF/mm$^2$. The second type of native capacitors is the MOS capacitors, they typically have high capacitive densities of about 3 to 20 nF/mm$^2$ [69]. MOS capacitances also have their drawbacks, the capacitance value is non-linear and depends on the voltage across it, the parasitic resistance is relatively high, and the gate current leakage is high in modern processes.

The non-native capacitors are deep-trench capacitors which have capacitance densities of about 100 nF/mm$^2$ [70] and Metal-Insulator-Metal (MIM) capacitors. MIM capacitors come standard in many modern deep-submicron technologies. The capacitance densities of MIM capacitors is in the range of 1 to 2 nF/mm$^2$ with low parasitic resistances. They are also compatible with placing circuits underneath them [69]. MIM capacitors are also preferred in higher frequencies [5].

### 5.2.3 MOSFET

Traditional implementations had only a single MOSFET, while a diode was used instead of the PMOS. However, a diode introduces a forward voltage drop of around 0.6 V, where the power loss $P_D$ due to this drop has a linear dependence on the current flowing from anode to cathode. On the other hand, $r_{DS}$ of a MOSFET depends on the gate to source voltage applied, along with the size of the channel. The power loss $P_{rDS}$ due to $r_{DS}$ has a quadratic dependence on the current flowing from the drain to the source. For a MOSFET with a certain $r_{DS}$, $P_{rDS}$ will be lower than $P_D$ for a certain current threshold. This threshold value can be increased by decreasing $r_{DS}$, while the $P_D$ is fixed by the constant voltage drop.

The previous discussion does not take dynamic power losses into consideration. For a MOSFET these include the losses due to charging and discharging intrinsic capacitors, and the finite switching times. For a diode, these include the junction capacitances and the reverse recovery time. Since the focus of this work is integrated converters, the range of input and output voltages is relatively low, therefore, power losses will be minimized using a MOSFET switch instead of a diode.
CHAPTER 5. MODELLING OF INTEGRATED DC-DC CONVERTERS

Static power dissipation

Since the MOSFET acts as a switch, it behaves as a resistor, where \( r_{DS} \) for an NMOS is approximated by [71]

\[
r_{DSn} = \frac{1}{g_{DSn}} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)},
\]

(5.50)

and a PMOS by

\[
r_{DSP} = \frac{1}{g_{DSP}} = \frac{1}{\mu_p C_{ox} \frac{W}{L} (V_{SG} - |V_t|)}.
\]

(5.51)

From (5.50) and (5.51), it can be seen that \( r_{DS} \) is inversely proportional to the \( W/L \) ratio. The value of \( L \) should be minimized, and whenever the maximum voltage in the converter permits, should be the minimum allowed by the fabrication technology. The value of \( W \) should ideally be increased in order to minimize the on resistance and the power dissipation. However, as will be shown next, increasing the MOSFET size increases the capacitance and in turn the dynamic power dissipation [5].

The power losses in \( M_1 \) and \( M_2 \) are given by (5.52) and (5.53) respectively

\[
P_{rDS1} = r_{DS1} I_{M1,RMS}^2,
\]

(5.52)

\[
P_{rDS2} = r_{DS2} I_{M2,RMS}^2,
\]

(5.53)

where \( I_{M1,RMS} \) and \( I_{M2,RMS} \) were found in (5.43) and (5.44) in DCM and (5.45) and (5.46) in CCM, respectively.

Dynamic power dissipation

Fig. 5.10 shows an NMOS with its parasitic capacitances: the gate to source capacitance \( (C_{GS}) \), the gate to drain capacitance \( (C_{GD}) \), the gate to substrate capacitance \( (C_{GS}) \), the drain to substrate capacitance \( (C_{DB}) \), and the source to substrate capacitance \( (C_{SB}) \). These capacitances can be categorized into four types as follows:

1. Oxide capacitance between the gate and the channel \( C = W L C_{ox} \).
2. Depletion capacitance between the channel and the substrate \( C = W L \sqrt{\frac{qE_s N_{sub}}{4\Phi_F}} \).
3. Overlap capacitances from the gate to the source and drain \( C = W L_{ov} C_{ox} \).
4. Junction capacitances from the source and drain to the substrate.

The power loss resulting from these capacitances is given by

\[ P_C = f_{SW} CV_{\text{swing}}^2. \]  

(5.54)

where \( V_{\text{swing}} \) is the voltage swing over which the capacitor is charged and discharged, and \( C \) in the triode region of operation is given by the gate capacitance which is equal to \( C_{GS} = C_{GD} \approx \frac{1}{2} WL_{ox} + W L_{ov} C_{ox}. \)  

(5.55)

**Finite switching times**

The third power loss associated with MOSFETs is caused by the finite switching times needed for a MOSFET to fully turn on or off. During these transients a voltage across and current through the MOSFET exist. The power loss can be calculated by

\[ P_{Tsw} = f_{SW} \int_0^{t_{SW}} i_{MOS}(t) V_{DS}(t) \, dt. \]  

(5.56)

where \( t_{SW} \) denotes the time during which the switching transient occurs. The finite switching times of a MOSFET are mainly due to the output resistance of the driver charging and discharging the parasitic gate capacitance of the MOSFET.
5.2.4 Interconnections

Interconnections play an important role in determining the conversion efficiency and output voltage ripple of a dc-dc converter. The on-chip interconnects introduce additional parasitic resistance, capacitance, and inductance. The parasitic inductance is usually small enough to be neglected. The parasitic resistance and capacitance on the other hand, are significant and largely dependent on the chip layout. The interconnect at the input and output are more complex since they comprise bondwires for the connection with the package, and on-chip metal-tracks to connect to the converter circuitry.

The parasitic series resistance $R_{Vin}$ of the bondwires and metal-tracks at the input introduce an input voltage ripple $\Delta V_{IN}$. This in turn, introduces a power loss at this input, $P_{RVin}$, which is given by

$$P_{RVin} = R_{Vin}I_{M1,RMS}^2$$

for a boost converter, and

$$P_{RVin} = R_{Vin}(I_{M1,RMS}^2 + I_{M2,RMS}^2)$$

for a buck converter.

The effect of this resistance is usually taken into account along with the resistance of the input source. An on-chip input decoupling capacitor is usually introduced to reduce $\Delta V_{IN}$. It should be noted that the series parasitic resistance of this capacitor should be kept minimum as it influences the effectiveness of the decoupling capacitor. In some cases, an input off-chip decoupling capacitor is introduced to avoid excessive voltage swing due to long PCB tracks. $\Delta V_{IN}$ also has a negative effect on $\Delta V_{OUT}$.

At the output of the converter, metal-track and bondwire interconnections also introduce a parasitic series resistance $R_{Vout}$. This resistance becomes more significant at higher values of $P_{OUT}$. The power loss associated with $R_{Vout}$ is given by

$$P_{RVout} = R_{Vout}\frac{V_{OUT,rms}^2}{R}.$$  \hspace{1cm} (5.59)

The design of integrated dc-dc converters highly depends on the fabrication technology being used. Technology parameters such as the minimum feature size and the oxide thickness highly affect the static and dynamic losses associated with the switches. Additionally, the number, thickness, and resistivity of the metal layers available have a direct impact on the quality factor of the inductors and the series parasitic resistance of the capacitors. Finally, the availability of MIM capacitors, along with their capacitance density and maximum operating voltage have to also be taken into account.
5.3 Efficiency model

The main resistive power losses were included in the second-order model introduced in Section 5.1. The most significant dynamic losses from Section 5.2 are integrated in the second-order model in this section, so as to calculate the final $V_{OUT}$ and the conversion efficiency $\eta$.

The additional dynamic losses will result in less power being transferred to the load, and larger dissipated power, therefore, they can be modelled as a resistive loss $R_{LOSS}$ in parallel to the load resistance $R$ at the output of the converter. The resulting load resistance $R_{LOAD}$ is given by

$$R_{LOAD} = R_{LOSS} \parallel R.$$  \hspace{1cm} (5.60)

The resulting load resistance is smaller than the initial load resistance not taking the dynamic losses into consideration. Consequently, a lower $V_{OUT\text{rms}}$ is achieved in this case. The resulting output voltage $V'_{OUT\text{rms}}$ is calculated by [5]

$$V'_{OUT\text{rms}} = \sqrt{R_{LOAD} P'_{OUT}} = \sqrt{R_{LOAD} (P_{OUT} - P_{LOSS})},$$  \hspace{1cm} (5.61)

where $P'_{OUT}$ is the real output power taking the dynamic losses into account, $P_{OUT}$ is the output power calculated with taking only the resistive losses into consideration, and $P_{LOSS}$ is given by

$$P_{LOSS} = P_C + P_{Tsw} + P_{RVout} + P_{Cbuffer} + P_{SCbuffer},$$  \hspace{1cm} (5.62)

where $P_C$ is the power loss due to the parasitic capacitances of the MOSFETs given by (5.54), $P_{Tsw}$ is the power loss due to finite switching times of the MOSFETs given by (5.56), $P_{RVout}$ is the power loss due to the parasitic resistance of the interconnect at the output given by (5.59), $P_{Cbuffer}$ is the power loss due to the parasitic capacitances of the buffers driving the MOSFETs, and $P_{SCbuffer}$ is the power loss due to the short-circuit current of the buffers. The efficiency is then given by [5]

$$\eta = \frac{V'_{OUT\text{rms}}^2}{R_{LOAD} (P_{LOSS} - P_{RL} - P_{RC} - P_{RCP} - P_{rDS1} - P_{rDS2} - P_{RVin})},$$  \hspace{1cm} (5.63)

where $P_{RL}$ is given by (5.42), $P_{RC}$ is given by (5.47), $P_{RCP}$ is given by (5.51), $P_{rDS1}$ is given by (5.52), $P_{rDS2}$ is given by (5.53), and $P_{RVin}$ is given by (5.57).
Design trade-offs

Several trade-offs arise in the design process of an integrated dc-dc converter. In the discussion to follow four design trade-offs are explained:

- A larger inductance requires lower switching frequency for a given filter capacitance. That is because a larger inductance allows for more energy to be stored per cycle as it allows for longer charge time, $t_{ch}$. However, increasing the inductance would, on the other hand, introduce higher series parasitic resistance and substrate capacitance which add to the losses. While decreasing the inductance require increasing the frequency to accommodate for the limited energy being stored in the inductor, hence, increasing the switching losses.

- Extremely low or high inductance values affect the efficiency of the converter negatively. For low values of inductance the drop in efficiency is due to high switching losses. On the other hand, for high values of inductance, the efficiency drops due to higher series parasitic resistance and substrate capacitance. Increasing the filter capacitance for the same value of inductance would increase the efficiency and decrease the ripple of the output voltage.

- The value of the inductance also affects the conduction mode of the converter. High values of inductance are associated with higher $t_{ch}$ and thus the converter will tend to work in CCM, whereas, low values of inductance will make it work in DCM.

- Lower values of capacitance require higher switching frequencies, for the same $\Delta V_{OUT}$. A higher value of capacitance would result in a higher efficiency and lower $\Delta V_{OUT}$. Also, for a lower value of $R_C$ a lower $C$ is adequate to achieve a certain $\Delta V_{OUT}$ and efficiency.

5.4 Temperature effects

An effect that should be taken into account is the influence of the temperature on the performance of the converter. Since a converter will have an efficiency lower than 100%, the total dissipated power $P_{loss}$ will cause the temperature of the converter to rise above the ambient temperature. For integrated converters, it is reasonable to assume that this temperature increase will be uniformly distributed over the entire chip, since the thermal conductivity $\lambda_{th}$ of silicon is fairly high ($\lambda_{th, Si} = 150 \text{ W/(m . K)}$) \[5\].

The temperature increase $\Delta T$ of a converter can be approximated by

$$\Delta T = \gamma P_{loss},$$  \hspace{1cm} (5.64)
where $\gamma$ is the thermal resistivity of the chip die to the ambient. When the die is mounted onto a PCB, the value of $\gamma$ can be in the order of 250 K/W [74]. This becomes significant for large values of $P_{\text{loss}}$.

### 5.4.1 Inductor

An on-chip inductors has an associated series parasitic resistance $R_L$, which has a positive temperature coefficient (PTC). This means that the value of this resistance increases as a function of temperature. For a certain temperature increase $R_L$ is calculated as

$$R_L(T + \Delta T) = R_L(T)(1 + \alpha \Delta T), \quad (5.65)$$

where $R_L(T)$ is the resistance at the ambient temperature $T$, $R_L(T + \Delta T)$ is the resistance at temperature $T + \Delta T$, and $\alpha$ is the resistance temperature coefficient of the metal layer (for copper $\alpha = 4 \times 10^{-3}$ K$^{-1}$). For integrated inductors the temperature of the windings will be evenly distributed and approximately equal to the chip die temperature [5], [75]. Therefore, an increase in the temperature of the chip due to $P_{\text{loss}}$ will result in an increase in $R_L$, which will in turn increase $P_{RL}$. This effect is accentuated at higher values of $P_{OUT}$.

### 5.4.2 Power switches

Power switches are affected by the temperature increase in both the on and off states. When the MOSFET is on its on-resistance also exhibits a positive temperature coefficient. The reason behind this dependence is due to that fact that the threshold voltage increases and the mobility decreases with increasing temperature [76]. The first order effect can be described by

$$R_{DS}(T + \Delta T) = R_{DS}(T)(1 + \alpha_{\text{mos}} \Delta T), \quad (5.66)$$

where $\alpha_{\text{mos}}$ can be extracted through simulations and is assumed to be equal for both NMOS and PMOS and is about $3 \times 10^{-3}$ K$^{-1}$.

In the off state the drain-to-source leakage current $I_{\text{leak}}$ of a MOSFET increases as a function of temperature. For modern technologies $I_{\text{leak}}$ is in the range of a few $\mu$A at room temperature. Upon increasing the temperature by 100 K the current increases by two orders of magnitude. The power loss due to this can then be neglected at the output power range of this work since it will be in the order of a few $\mu$W.
If the temperature effects are to be taken into account in the model the resistances are to be replaced by the temperature dependent resistances introduced in (5.65) and (5.66) into the conversion efficiency model developed in the previous section.

5.5 Electromagnetic Interference (EMI)

At the output of a converter, the parasitic series resistance associated with the filter capacitor can cause steep transients at the transition between the charge and discharge phases which increases the effective amplitude of $\Delta V_{OUT}$. In a boost converter, those transients are due to the fact that the current towards the capacitor is discontinuous. Consequently, the odd harmonics have a significantly larger amplitude in comparison to the case with an ideal filter capacitor. This presents a problem in terms of EMI towards the load and the neighbouring circuits.

In a buck converter the current towards the filter capacitor is continuous. Therefore, the potential EMI problems are usually fewer than in a boost converter. The parasitic series resistance of the capacitor still introduces discontinuities in $V_{OUT}$, which is observed through an increase of both the amplitudes of odd and even harmonics.

For a Pulse-Width-Modulated (PWM) converter, since it operates at a certain constant frequency, EMI is well defined and predictable. PWM can be beneficial if the switching frequency is higher than the signal band of the application. For a Pulse-Frequency-Modulated (PFM) converter, EMI is more difficult to predict since the switching frequency is a function of the output power.

At the input of a converter, the input-current ripple is the main reason for EMI. This is more pronounced for boost converters operating in DCM since the current becomes discontinuous and pulsating. For these reasons it is preferable for some applications to use other converter types, such as Cuk and SEPIC in order to achieve continuous or zero-ripple input current using coupled inductors. Another solution is to implement an EMI filter at the input of the converter, which can be a decoupling capacitor [5], [77], an LC network [78], or coupled inductors forming a smoothing transformers [79], [80]. In Chapter 8 we investigate a boost configuration that reduces EMI.
5.6 Summary

In this chapter, a detailed mathematical model that takes all resistive losses into consideration was introduced in the first section for a boost and a buck converters. The power losses associated with each component were discussed in the second section. Finally, a full model flow with the different trade-offs was presented in the third section. In the next chapter, resistance modelling of inductors will be discussed in more detail. Since inductors are the main energy storage components in a converter, it is crucial to accurately model their resistance in order to eventually minimize their power losses and optimize their performance.
Chapter 6

Modelling of the resistance of on-chip inductors

Planar on-chip integrated inductors are constructed by connecting metal segments to form a spiral shape. Traditionally, mask generation systems were only able to generate Manhattan-style layouts (i.e. layouts with only 90° angles) and hence only square spirals were possible. As the fabrication technology advanced, more shapes became possible from square to circular spirals. The approach taken to calculate the total series parasitic resistance is by counting the total number of squares in a spiral, however, since the current tends to take the shortest path, current crowding will occur around the inside corner increasing the current density distribution. Therefore, the resistance of corners have to be treated in a different way. In this chapter, the resistance of corners is calculated using the Schwarz–Christoffel transformation. In Section 6.1 the square inductor is considered as a special case and the corner resistance is calculated. A generalized approach is proposed in Section 6.2 and a design example is shown in Section 6.3

6.1 Square spiral inductors

The resistance of a polygon conductor can be calculated by breaking up the shape into smaller polygons and determining the dominant direction of current flow [81][82]. Although, this approximation is simple, the results are not very accurate, especially when the current highly spreads from the dominant flow direction. Also, this method assumes that the current spreads at a 45° angle which gives a worst-case error of 10%. The extracted resistance using the algorithm of [82] for a corner square like the one shown in Fig. 6.1 is equal to 0.5 squares.
Alternatively, conformal mapping, which has been originally used for determining resistance in thin strip conductors [83-86], is a more accurate approach. This work will specifically use Schwarz–Christoffel mapping, which is a transformation that can be applied to generalized polygon geometries by mapping a 90° bent conductor from the Z-plane to a straight rectangular strip in the Z1-plane, using the W-plane [84,87]. Fig. 6.2 shows the transformation steps. We start with the special case of the 90° angle and then we generalize the expression for an arbitrary angle.

The transformation maps the bent conductor into a rectangular conductor where the resistance is easier to calculate. In the Z-plane, the width \( w \) of the conductor is fixed, as is usually the case for on-chip inductors. As can be seen in Fig. 6.2, the current density increases around the inner corner. In the Z1-plane the current is flowing parallel to the X1 axis. Therefore, X1 represents the potential function and Y1 the stream function. For example, the straight line c-d is an equipotential line (i.e. c and d have the same X1 and hence the same potential). Equation (6.1) maps a 90° bent conductor from Z-plane to its W-plane and (6.2) from W-plane into the rectangular strip in the Z1-plane. Both equations are simplified versions of the general equations introduced in [84,88,89], as the width is uniform and the inside corner is a sharp 90° one.

\[
\begin{align*}
z &= 2 \left( \cos^{-1} (1 - w) + \cosh^{-1} \left( \frac{1}{1 - w} \right) \right), \\
w &= 1 - e^{-z1}.
\end{align*}
\]  

(6.1)

Solving both equations

\[
\begin{align*}
z &= 2 \left( \sec^{-1} (e^{z1}) + \cosh^{-1} (e^{z1}) \right),
\end{align*}
\]  

(6.3)
where \( z_1 = x_1 + iy_1 \). The next step is to get expressions for \( x \) and \( y \), where \( x = Re(z) \) and \( y = Im(z) \), assuming that the width of the rectangular strip in the \( Z_1 \)-plane is \( \pi \). The expressions for \( x \) and \( y \) are given by (6.4) and (6.5), respectively

\[
x = \ln \left( e^{2x_1} + \sqrt{(e^{2x_1} - 1)^2 - 2e^{x_1} \sqrt{(e^{2x_1} - 1)^2}} \cos \left( \frac{1}{2} \left( \arg(-e^{x_1} - 1) + \arg(1 - e^{x_1}) \right) \right) \right)
- 2 \arg(\sqrt{1 - e^{-2x_1} - ie^{-x_1}}) + \pi,
\]

(6.4)

\[
y = \ln \left( e^{-2x_1} + \sqrt{e^{-4x_1}(e^{2x_1} - 1)^2 - 2e^{-x_1} \sqrt{e^{-4x_1}(e^{2x_1} - 1)^2}} \sin \left( \frac{1}{2} \arg(1 - e^{-2x_1}) \right) \right)
+ 2 \arg(\sqrt{e^{2x_1} - 1 - e^{x_1}}).
\]

(6.5)

The problem then simplifies to finding the resistance between two equipotential lines in the \( Z_1 \)-plane which coincide with the ends of the \( 90^\circ \) bent conductor of the \( Z \)-plane. These two equipotentials only approach straight lines in the \( Z \)-plane as the length of each side of the segment approaches \( \infty \). The last step is to find the equivalent number of squares \( n_s \) of the bent strip by taking the limits as \( x_1 \) approaches \( \infty \) and \( -\infty \)

\[
n_s = \frac{x_l + y_l}{w} + \lim_{x_1 \to \infty} \left( \frac{x_1}{\pi} - \frac{x}{w} \right) - \lim_{x_1 \to -\infty} \left( \frac{x_1}{\pi} + \frac{y}{w} \right),
\]

(6.6)

where \( x_l \) and \( y_l \) are the lengths of the bent strip on the \( x \) and \( y \) directions, respectively. It can be shown that when the width \( w_1 \) of the straight strip is \( \pi \), the original width \( w \) is \( 2\pi \). Solving both limits results in

\[
n_s = \frac{x_l + y_l}{w} - \frac{2 \ln(2) + \pi}{2\pi} - \frac{4 \ln(2) + 2\pi}{4\pi},
\]

(6.7)

which corresponds to a corner coefficient \( c = 1 - 2 \ln(2)/\pi = 0.558729 \). The term \( (x_l + y_l)/w \) should be at least 6 (i.e. 3 squares on each side of the corner element) so that the equipotential lines can be assumed straight near the ends of the bent strip, in this case the resistance of the corner matches the calculated value to six decimal places \[84, 86\].

The equivalent number of squares for a square spiral inductor is

\[
n_s = \sum_{j=1}^{n} \frac{4 \left( (2j - 1) \hat{w} - (2j - 2) \hat{s} \right)}{\hat{w}} - 4 \left( 1 - c \right),
\]

(6.8)

where \( n \) is the number of turns, \( \hat{w} = w/d_{out} \) is the normalized segment width, \( \hat{s} = s/d_{out} \) is the
Figure 6.2: Conformal mapping of a 90° bent conductor in the Z-plane (top) transformed into a rectangular strip in the Z1-plane (bottom), by means of W-plane (middle).
normalized spacing between segments, and $c$ is the corner coefficient calculated above. Finally, using (4.9) the total value of the series parasitic resistance is obtained.

A limit case is when two consecutive bends with only a single square in between (not relevant for practical integrated inductors) as shown in Fig. 6.3. With the same procedure, it can be shown that the value of the corner coefficient above is an upper bound value, with a lower bound of $0.55232$ [85].

### 6.2 Polygon spiral inductors

As the angles of the bends increase, the current crowding around the inner corners of the inductor decreases until it disappears at $180^\circ$ (i.e. a rectangular strip). The Schwarz-Christoffel transformation can be applied to polygons with arbitrary angle bends. For any angle $0 < \theta < 180^\circ$, setting $P$ and $Q$ that satisfy

$$
\frac{P}{Q} = 1 - \frac{\theta}{\pi},
$$

the transformation is defined as [89]

$$
\begin{cases}
  z = 4Q(i \cos \theta - \sin \theta) \int \frac{h^{Q-(P+1)}}{h^2-1} \, dh \text{ with } h = \left(\frac{w+1}{w-1}\right)^{\frac{1}{\bar{Q}}}, \\
  w = -e^{-z1}
\end{cases}
$$

The equations can be reduced to a single equation of the form $z(z1)$, where $z = x + iy$ and $z1 = x1 + iy1$. The transformation can be used to map a strip bent at a random angle $\theta$ from the $Z$-plane into a rectangular strip in the $Z1$-plane by means of the $W$-plane. Once expressions for $x$
Table 6.1: Corner coefficients for different angles.

<table>
<thead>
<tr>
<th>Angle [°]</th>
<th>Corner coefficient [□]</th>
<th>Previously reported coefficients [□]</th>
</tr>
</thead>
<tbody>
<tr>
<td>90°</td>
<td>0.558729</td>
<td>0.5 [82], 0.525 [90], 0.5587 [84], 0.6 [92], 0.65 [93]</td>
</tr>
<tr>
<td>120°</td>
<td>0.410795</td>
<td>–</td>
</tr>
<tr>
<td>135°</td>
<td>0.325186</td>
<td>0.25 [82]</td>
</tr>
<tr>
<td>175°</td>
<td>0.042627</td>
<td>–</td>
</tr>
</tbody>
</table>

and \( y \) are obtained, the limits as \( x_1 \) approaches \( \infty \) and \( -\infty \) can be calculated leading to the value of the resistance of the corner.

The corner coefficient for an arbitrary angle \( \theta \) is expressed as

\[
c = \frac{2}{\pi} \int_{1}^{\infty} \frac{1}{u} \left( 1 - \left( \frac{u - 1}{u + 1} \right)^{1 - \frac{\theta}{\pi}} \right) du. \tag{6.11}
\]

Two cases for a hexagonal and octagonal spirals, corresponding to \( \theta \) of 120° (Fig. 6.4(a)) and 135° (Fig. 6.4(b)), respectively, were solved and their corner coefficients are reported in Table 6.1. The equivalent number of squares for a hexagonal spiral inductor is

\[
n_s = 6n \sum_{j=1}^{n} \frac{6 - (7 + 2j)\hat{w} + (5 - 2j)\hat{s}}{6\sqrt{3}\hat{w}} + c_{120}, \tag{6.12}
\]

where \( c_{120} \) is the corner coefficient of the 120° case and \( \hat{w} \) is \( w/d_{out} \). Similarly, \( n_s \) for an octagonal spiral inductor is

\[
n_s = 8n \sum_{j=1}^{n} \frac{(\sqrt{2} - 1)(4 - (9 + j)\hat{w} - (1 + j)\hat{s})}{4\hat{w}} + c_{135}, \tag{6.13}
\]

where \( c_{135} \) in this case is the corner coefficient for 135°. The number of squares found in (6.12) or (6.13) is substituted into (4.9) to get the total parasitic resistance.

The curved metal traces of a circular spiral can be approximated with a series of straight segments. In this paper we used 72 metal segments per turn, which translates to 175° angles between adjacent segments. Utilizing the same transformation, the corner coefficient value is also reported in Table 6.1 [20].
6.3 Example implementations in CMOS

Results from the resistance expressions derived above are compared to simulation results from ASITIC [36]. All inductors are designed using the top metal layer (M6) of a standard 0.18-μm CMOS technology (with no thick metal option), have an outer diameter $d_{out} = 400$ μm, have a spacing between traces $s = 2$ μm, and operate at 100 MHz.

The first two examples consider a square inductor and a hexagonal inductor with trace width $w = 15$ μm. Figs. 6.5 and 6.6 show how their parasitic resistances change with the number of turns from 2 to 12. The calculation results (solid lines) are compared to the simulation results from ASITIC (dashed lines) and display a maximum absolute error of 3.4% and 3.5%.

The other two examples consider an octagonal inductor and a circular inductor (approximated with 72 segments per turn) with $n = 5$ turns. Figs. 6.7 and 6.8 show how their parasitic resistances change with the trace widths from 5 to 40 μm. The calculation results (solid lines) are compared to the simulation results from ASITIC (dashed lines) and display a maximum absolute error of 3.9% and 3.8%.

6.4 Summary

In this chapter, the parasitic resistance for different geometrical shapes was derived using the Schwarz–Christoffel transformation. A design example was also provided to show the accuracy of the expressions proposed. In the next chapter, the relationship between the inductance time-constant ratio $L/R_L$ will be introduced and optimized.
CHAPTER 6. MODELLING OF THE RESISTANCE OF ON-CHIP INDUCTORS

Figure 6.5: Resistance of a square inductor, derived expression (solid) and ASITIC simulations (dashed), $d_{out} = 400 \, \mu m$, $w = 15 \, \mu m$, $s = 2 \, \mu m$, $f_{SW} = 100 \, MHz$, process: 0.18 $\mu m$, metal: M6.

Figure 6.6: Resistance of hexagonal inductor, derived expression (solid) and ASITIC simulations (dashed), $d_{out} = 400 \, \mu m$, $w = 15 \, \mu m$, $s = 2 \, \mu m$, $f_{SW} = 100 \, MHz$, process: 0.18 $\mu m$, metal: M6.
Figure 6.7: Resistance of an octagonal inductor, derived expression (solid) and ASITIC simulations (dashed), \( d_{out} = 400 \, \mu m \), \( n = 5 \), \( s = 2 \, \mu m \), \( f_{SW} = 100 \, MHz \), process: 0.18 \( \mu m \), metal: M6.

Figure 6.8: Resistance of a circular inductor, derived expression (solid) and ASITIC simulations (dashed), \( d_{out} = 400 \, \mu m \), \( n = 5 \), \( s = 2 \, \mu m \), \( f_{SW} = 100 \, MHz \), process: 0.18 \( \mu m \), metal: M6.
Chapter 7

Inductance time-constant ratio optimization

This chapter starts by investigating the relationship between the conversion efficiency and the inductor time-constant ratio $L/R_L$ [94], in order to show the significance of optimizing it in Section 7.1. In Section 7.2, the effect of geometrical parameters on $L/R_L$ is explained along with introducing a shape coefficient $k$. In Section 7.3, an algorithm for finding the trade-off envelope for the inductance versus parasitic resistance is developed, that is valid for the range of resistances of interest for maximizing the conversion efficiency (i.e. a few Ohms). Section 7.4 shows the simulation results using the TSMC 65 nm technology. The results from the proposed trade-off envelope are compared to those of ASITIC [39], and show errors below 3%. A design example comparing three identical boost converters each using a different inductor is also included and shows an improvement in conversion efficiency of around 5% for the same area, which is in good agreement with the analysis.

7.1 Efficiency and time-constant ratio

7.1.1 Boost converter

An efficiency model based on the discussion in Chapter 5 is briefly introduced. The total power loss can be expressed as

$$\eta_{CCM} = \frac{P_{OUT}}{P_{OUT} + P_{Loss}}, \quad (7.1)$$

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where $P_{\text{OUT}}$ is the output power and $P_{\text{Loss}}$ is the power dissipated in the parasitic elements. The latter is divided into the conduction power loss of parasitic resistors and the switching power loss of parasitic capacitors. The conduction losses are evaluated based on an inductor with a ripple current $\Delta i_L$ [55]. The root-mean-square inductor current is evaluated as follows

$$I_{L,RMS} = \sqrt{\frac{1}{T} \int_0^T i_L^2(t) \, dt} = \sqrt{\frac{1}{T} \left( \int_0^{DT} (I_{\text{min}} + \frac{\Delta i_L}{T} t)^2 \, dt + \int_{DT}^T (I_{\text{min}} + \Delta i_L \frac{T - t}{DT})^2 \, dt \right)}, \quad (7.2)$$

where $I_{\text{min}}$ is equal to $I_L - \Delta i_L/2$. Solving (7.2)

$$I_{L,RMS} = \sqrt{\frac{(V_{\text{OUT}} - V_{\text{IN}})^2 V_{\text{IN}}^2}{12 f^2 L^2 V_{\text{OUT}}^2} + \frac{V_{\text{OUT}}^2 I_{\text{OUT}}^2}{V_{\text{IN}}^2}}. \quad (7.3)$$

where $I_{\text{OUT}}$ is the dc current through the load resistor.

The total power loss is then calculated as

$$P_{\text{Loss}} = f_{\text{SW}} V_{\text{OUT}}^2 (C_n + C_p) + I_{L,RMS}^2 (R_L + D r_{DSn} + (1 - D) r_{DSP} + (1 - D) R_C) - I_{\text{OUT}}^2 R_C, \quad (7.4)$$

where $C_n$ is the NMOS parasitic capacitance and $C_p$ is the PMOS parasitic capacitance, $R_L$ is the parasitic resistance of the inductor, $r_{DSn}$ and $r_{DSP}$ are the parasitic resistances of the NMOS and PMOS respectively, and $R_C$ is the parasitic resistance of the filter capacitor.

The expression (7.4) becomes

$$P_{\text{Cond}} = I_{L,RMS}^2 (R_L + D r_{DSn} + (1 - D) r_{DSP} + (1 - D) R_C) - I_{\text{OUT}}^2 R_C, \quad (7.5)$$

when neglecting the capacitive losses term and focusing on the conduction losses, because in a practical fully-integrated dc-dc converter the size of the switches can be optimized to minimize the switching losses [10]. Furthermore, typical designs have $r_{DSn} \approx r_{DSP}$ and $R_C \ll r_{DSn}$. Therefore (7.5) can be simplified as

$$P_{\text{Cond}} \approx (R_L + r_{DSn}) I_{L,RMS}^2. \quad (7.6)$$

Using (7.6) and (7.3), the expression for the conversion efficiency (7.1) can be rewritten as

$$\eta \approx \left(1 + \frac{I_{\text{OUT}}}{V_{\text{OUT}}} \left(\frac{(V_{\text{OUT}} - V_{\text{IN}}) V_{\text{IN}}}{2 \sqrt{3} f_{\text{SW}} V_{\text{OUT}} I_{\text{OUT}}} \right)^2 + \left(\frac{V_{\text{OUT}}}{V_{\text{IN}}} \right)^2 \right) (R_L + r_{DSn})^{-1}. \quad (7.7)$$
Figure 7.1: The maximum efficiency versus the output voltage gain for different $f_L/R_L$ ratios.

Differentiating to find the maximum of this expression results in

$$\hat{\eta} = \left(1 + \frac{1 - V_{IN}/V_{OUT}}{\sqrt{3} f_{SW} L/(R_L + r_{DSn})}\right)^{-1},$$

(7.8)

at

$$I_{OUT} = \frac{V_{IN}^2 (V_{OUT} - V_{IN})}{2\sqrt{3} f_{SW} L V_{OUT}^2}.$$  

(7.9)

Considering that the total area of the switches is usually between 1% and 10% that of the inductor, the on resistance of the switches is typically between five and ten times smaller than the series parasitic resistance of the inductor [10], [9]. Therefore, the peak efficiency can then be approximated by

$$\hat{\eta} \approx \left(1 + \frac{1 - V_{IN}/V_{OUT}}{\sqrt{3} f_{SW} L/R_L}\right)^{-1},$$

(7.10)

where the inductance time-constant ratio $L/R_L$ is highlighted.

The relationship between the maximum achievable conversion efficiency, $\hat{\eta}$, and the voltage gain is plotted in Fig. 7.1. The input voltage is kept constant at 1 V, while the output voltage changes from 1 to 2.4 V. Four curves each with a different normalized $L/R_L$ ratio are plotted. The solid black curve represents $f_L/R_L = 1$, the dashed curve represents $f_L/R_L = 0.7$, the dotted
curve represents $f L / R_L = 0.4$, and the dash-dotted curve represents $f L / R_L = 0.1$. When the inductance time-constant ratio increases, an improvement in the efficiency can be achieved as shown.

Similar analysis for the efficiency of the boost converter in DCM was conducted, and the same trend was observed. Looking at the analytical results of this section, it is worth mentioning that the proper design of integrated inductors is one of the critical aspects in increasing the efficiency of the boost converter. Specifically, the inductance time-constant ratio plays a key role in determining the overall conversion efficiency of the boost converter. Therefore, when designing an integrated dc-dc converter, the integrated inductor has to be designed so that the $L / R_L$ ratio for a specific given area and switching frequency is the highest that the used technology allows.

### 7.1.2 Buck converter

A buck dc-dc converter operating in CCM is briefly discussed to show that the resistance of the inductor has the same effect on the conversion efficiency. The main losses are expressed as follows. The conduction power loss associated with $M_1$ and $M_2$ are given by

\[
P_{rDSP} = r_{DSP} I_{PMOS,RMS}^2 = r_{DSP} D I_{OUT}^2, \tag{7.11}
\]

\[
P_{rDNS} = r_{DNS} I_{NMOS,RMS}^2 = r_{DNS} (1 - D) I_{OUT}^2. \tag{7.12}
\]

The capacitive switching losses associated with $M_1$ and $M_2$ are

\[
P_{SWp} = C_p f_{SW} V_{IN}^2, \tag{7.13}
\]

\[
P_{SWn} = C_n f_{SW} V_{IN}^2. \tag{7.14}
\]

The loss due to the series parasitic resistance of the inductor is given by

\[
P_{RL} = R_L I_{L,RMS}^2 = R_L I_{OUT}^2. \tag{7.15}
\]

The loss due to the series parasitic resistance of the capacitor is

\[
P_{RC} = R_C I_{C,RMS}^2 = \frac{R_C \Delta i_C^2}{12} = \frac{R_C V_{OUT}^2 (1 - D)^2}{12 f_{SW} L^2}. \tag{7.16}
\]

Taking only the conduction losses into account results in
\[ P_{\text{Cond}} = I_{\text{OUT}}^2 (R_L + D r_{DSp} + (1 - D) r_{DSn}) + \frac{R_C V_{\text{OUT}}^2 (1 - D)^2}{12 f_{SW}^2 L^2} \]  

(7.17)

Using (7.17), the expression for the conversion efficiency (7.1) is rewritten as

\[ \eta \approx \left( 1 + \frac{I_{\text{OUT}}}{V_{\text{OUT}}} (R_L + r_{DSn} + \frac{R_C V_{\text{OUT}}^2 (V_{\text{IN}} - V_{\text{OUT}})^2}{12 f_{SW}^2 P_{\text{OUT}}^2 L^2 V_{\text{IN}}^2}) \right)^{-1} \]  

(7.18)

Differentiating (7.18) to find the maximum efficiency results in

\[ \hat{\eta} = \left( 1 + \frac{1 - V_{\text{OUT}}/V_{\text{IN}}}{\sqrt{3} f_{SW} L/(R_L + r_{DSn})} \right)^{-1} \]  

(7.19)

at

\[ \hat{I}_{\text{OUT}} = \frac{V_{\text{OUT}} (V_{\text{IN}} - V_{\text{OUT}})}{2 \sqrt{3} f_{SW} L V_{\text{IN}}} \]  

(7.20)

Similar to (7.10) the peak efficiency can be approximated as

\[ \hat{\eta} \approx \left( 1 + \frac{1 - V_{\text{OUT}}/V_{\text{IN}}}{\sqrt{3} f_{SW} L/R_L} \right)^{-1} \]  

(7.21)

As can be seen from the previous expression the conversion efficiency is inversely proportional to the parasitic resistance of the inductance, similarly to the boost converter.

### 7.2 Geometrical considerations

When designing an inductor, typically the frequency of operation, the area, and the process parameters are given, therefore, the designer usually deals only with geometric parameters. As an example, consider a square inductor implemented in metal 9 of the TSMC 65-nm technology, with a side length of 500 µm, thickness of 3.4 µm, and a frequency of 100 MHz. The relationship between the inductance and the parasitic resistance when changing the width (blue curve), number of turns (red curve), and spacing (green curve) individually, while keeping the other two parameters fixed is shown in Fig. 7.2. The arrows in the figure point to the direction of increasing the corresponding variable. The parasitic resistance is on the x-axis, and the
inductance is on the y-axis. All combinations of spacing, number of turns, and width were simulated using ASITIC [36]. The spacing between segments is shown to have a negligible effect on the resistance compared to that of the number of turns or the width. Therefore the spacing should be chosen to be the minimum value of the used technology. The reasoning behind this is that, electrically, $s$ controls the oxide coupling capacitance and the mutual magnetic coupling coefficient. In addition, minimizing $s$ allows for maximizing the mutual magnetic coupling and reducing resistive losses by allowing wider segment widths. It should be noted here that $s$ also affects current constriction, hence, the minimum spacing available is used at low frequencies $\approx 500$ MHz, while at high frequencies proximity effects favour a larger value of spacing [45].

### 7.2.1 Factor $k$

In the simplest approximation, the inductance of a single-loop planar inductor is proportional to the area of the loop, and the series resistance to the perimeter [43]. For the isogonal octagon in Fig. [7.3] the area and the perimeter are given by

$$
\begin{align*}
A &= a^2 + 2\sqrt{2}ab + b^2 \\
P &= 4(a + b)
\end{align*}
$$

(7.22)
where $a$ is the longest side and $b$ the shortest (i.e. the case of $b = 0$ corresponds to a square, and $a = b$ to a regular octagon).

Observing that the outer diameter is $d = a + \sqrt{2}b$ and introducing the factor $h = b/a$, the area to perimeter ratio is

$$\frac{A}{P} = \frac{1 + 2\sqrt{2}h + h^2}{(1 + h)(1 + \sqrt{2}h)}\frac{d}{4}, \quad (7.23)$$

which has a maximum

$$\left.\frac{A}{P}\right|_{\text{max}} = 2\left(3 - \sqrt{2}\left(\sqrt{7 + 5\sqrt{2}} - 2\right)\right)\frac{d}{4} \approx 1.047\frac{d}{4}, \quad (7.24)$$

at

$$h = \frac{\sqrt{2 + 10\sqrt{2} - 2\sqrt{2} + 1}}{7} \approx 0.3128, \quad (7.25)$$

while $A/P = d/4$ at $h = 0$, i.e. for a square shown in Fig. 7.4(a) and $A/P = d/4$ at $h = 1$, i.e. for a regular octagon shown in Fig. 7.4(c). The relationship between $h$ and the area to perimeter ratio can be shown in Fig. 7.5.

As stated by (7.24), the area to perimeter ratio of an isogonal octagon with $h$ given by (7.25)
is about 5% larger than the area to perimeter ratios of the square or the regular octagon with the same outer diameter \( d \) (shown in Fig. 7.4(b)). Accordingly, it is hypothesized that the inductance time-constant ratio \( L/R_L \propto A/P \) can be maximized by changing the factor \( 0 < h < 1 \) while maintaining the same silicon area occupation (i.e. the same enclosing square) [95].

The same approach can be extended to multi-turn inductors. For polygonal Archimedean spirals, a factor \( k \) can be defined such that each short side is given by

\[
b = \left( ka - \frac{\sqrt{2}-1}{4}(w+s) \right)^+,
\]

where \( a \) is the preceding long side given by

\[
a = \frac{1}{1+k\sqrt{2}}.
\]

Fig. 7.9 shows example implementations of inductors with different values of \( k \) occupying the same square area and number of turns.

It is expected that the inductance time-constant ratio can be additionally maximized by optimizing the parameter \( k \). For optimizing \( k \) different simulations were performed using ASITIC for inductors of different areas, segment widths, and number of turns. In the first set of simulations inductors with three different segment widths: 26 \( \mu \)m (solid), 28 \( \mu \)m (dashed), and 30 \( \mu \)m (dot-dashed) and values of \( k \) ranging from 0 to 1 are simulated. All inductors have the same area of 500 \( \times \) 500 \( \mu \)m\(^2\), a spacing of 2 \( \mu \)m, and each is 4 turns. A total of 21 inductors for each \( w \) were designed and simulated with a step of 0.05 in \( k \). As shown in Fig. 7.6, the normalized inductance time-constant ratio is maximized in each of the three different cases for \( k = 0.55 \).
Figure 7.5: $h$ versus the area to perimeter ratio.

Figure 7.6: Factor $k$ versus inductor time-constant ratio for inductors with three different widths (26, 28, 30 μm) for 4 turns and an outer diameter of 500 μm.
Figure 7.7: Factor $k$ versus inductor time-constant ratio for inductors with width of 28 $\mu$m for 2 turns and an outer diameter of 250 $\mu$m.

Figure 7.8: Factor $k$ versus inductor time-constant ratio for inductors with width of 28 $\mu$m for 6 turns and an outer diameter of 750 $\mu$m.
Figure 7.9: Realizations of polygonal inductors with different $k$. 

(a) $k = 0$ (square)  
(b) $k = 0.2$  
(c) $k = 0.4$  
(d) $k = 0.6$  
(e) $k = 0.8$  
(f) $k = 1$ (regular octagon)
Since the area and number of turns are kept constant in the first set of simulations, the second set keeps the segment width constant while sweeping on the number of turns and total area. The first family of inductors features an area of $250 \times 250 \mu m^2$, a width of $28 \mu m$, spacing of $2 \mu m$, and 2 turns. 21 inductors with $k$ ranging from 0 to 1 were designed and simulated as shown in Fig. 7.7. The second family of inductors occupies an area of $750 \times 750 \mu m^2$, a width of $28 \mu m$, spacing of $2 \mu m$, and 6 turns, with $k$ ranging from 0 to 1 as shown in Fig. 7.8. Similarly to the first set of simulations, the normalized inductance time-constant ratio is maximized for $k = 0.55$.

Inductors with $n = 4$ and $n = 5$ turns enclosed in a rectangle of $0.2 \text{ mm}^2$ were simulated. The parameters of the TSMC 65-nm technology (CMN65GP) were used with $s$ kept at $2 \mu m$ and $w$ changed between $24 \mu m$ and $32 \mu m$. The optimal value for $k$ was also around 0.55. As expected, the optimized inductor shows improvement in $L/R_L$ of about 4% for the $n = 4$ case (Fig. 7.10), and about 6% for the $n = 5$ case (Fig. 7.11).

### 7.2.2 Geometrical limits

In order for the resistance to be calculated the number of squares of an inductor with a given area has to be formalized. All the geometrical-defining parameters ($d_{\text{out}}$, $d_{\text{avg}}$, $w$, and $s$) are normalized, by dividing each parameter by $d_{\text{out}}$, hence the outer diameter will always have a value of 1 and $d_{\text{avg}}$, $w$, and $s$ will always be smaller than 1. The total length takes into consideration the corner coefficient $c$ and the shape factor $k$. The general formula for calculating the total number
CHAPTER 7. INDUCTANCE TIME-CONSTANT RATIO OPTIMIZATION

Figure 7.11: Inductance versus resistance for 5-turns 0.2-mm² inductors: proposed shape in black, square in solid grey, and regular octagon in dashed grey.

of squares (the total length of an inductor divided by the segment width) of an inductor is given by

\[
l_{tot} = \frac{4n}{w} \left( a_x - \frac{(\sqrt{2}-1)}{2} \frac{(w+s)}{w} (i-1) \right) + \sum_{i=1}^{\max(0,4n-m)} (c_{90})
\]

\[
+ \sum_{i=1}^{\min(4n,m)} \left( a_x k - \frac{(\sqrt{2}-1)}{2} \frac{(w+s)(i-\frac{1}{2})}{w} + c_{135} \right),
\]

(7.28)

where \(a_x = a - \frac{2w}{1+\sqrt{2}}\), \(c_{135}\) is the corner coefficient for the 135°, \(c_{90}\) is the corner coefficient for the 90°, and \(m\) is given by

\[
m = \frac{1}{2} + 2(1+\sqrt{2}) \frac{ak}{w+s}.
\]

(7.29)

Fig. 7.12 provides an example to show the geometrical limitations for an inductor with a given area. In this example the relationship between the normalized pitch (segment width and spacing) and the number of turns is highlighted. For this example \(k = 0.55\). The limit on number of turns for a given pitch is represented by a black solid curve, as can be seen, when the pitch increases the maximum number of turns decreases. The grey tones represent the number of non-chamfered turns as follows: the darkest tone represents a spiral with all turns chamfered, the lighter tone is
a spiral with only the innermost turn square-shaped, and each lighter tone adds a square turn up to the white tone which has 4 square-shaped turns. The black dotted lines represent the typical range of integrated inductors used in dc-dc converters, with typical areas ranging from 0.04 to 0.64 mm$^2$, normalized pitches between 0.03 and 0.09, and turns between 2 and 8 \cite{6,9,36,49}.

### 7.2.3 Inductance and resistance limits

In order for the optimization algorithm to be developed, first, the upper and lower limits of the inductance and parasitic resistance values are to be determined for a given area, frequency, and processing technology. This is important in order to have a well-defined design space. The resistance is normalized by dividing it by the sheet resistance giving the total number of squares in an inductor. The inductance is also normalized by dividing it by $d_{\text{out}} \times \mu_1 \times \mu_0$. The minimum resistance occurs when the inductor has only a single turn, and the width is maximum, which is also a technology-based limit, and is given by

$$w = w_{\text{max}} \approx \frac{1}{2} d_{\text{out}} - s \land n = 1.$$  \hspace{1cm} (7.30)
The maximum resistance is found at the maximum number of turns that the outer diameter can fit combined with the minimum allowable segment width of the given technology which is usually equal to the minimum spacing

\[ w = w_{\text{min}} = s_{\text{min}} \land n = n_{\text{max}}. \]  

(7.31)

The minimum inductance occurs when the width is maximum and there is only one turn (7.30). The maximum inductance, on the other hand, is calculated by first taking the derivative of the inductance with respect to the number of turns from (4.7), \( \frac{\partial L(w, s, n)}{\partial n} \), equating it to zero and solving for \( n \). The second step is to substitute the expression for \( n \) in the inductance equation \( L(w, s, n) \Rightarrow L(w, s) \). Finally, \( w_{\text{min}} \) is substituted in the resulting expression which leads to the maximum inductance.

### 7.3 \( L/R_L \) trade-off

#### 7.3.1 Trade-off algorithm

The procedure to find the trade-off envelope for an inductor with a given area is the focus of this section. The procedure applies to inductors of different shapes. It is assumed that the frequency, silicon area, and technology are specifications to be chosen by the designer.

We start by defining the three main equations that will be used to find the trade-off envelopes. The first is the modified Wheeler inductance (4.7), which is of the form \( L(n, d_{\text{avg}}) \). The second is the resistance (4.9), which is of the form \( R_L(n, w, s, d_{\text{avg}}) \). The last is the average diameter (4.3), which is of the form \( d_{\text{avg}}(n, w, s) \).

First we study the relationship between the inductance and the parasitic resistance by plotting the normalized inductance \( L \) on the y-axis and normalized resistance \( R \) on the x-axis using two different approaches. The first approach is shown in Fig. 7.13. Each curve represents a specific \( n \) for an inductor with \( k = 0.55 \). This is achieved by solving the three equations for \( L \) and \( w \) and plotting \( L(R_L, n, s) \) where \( s = s_{\text{min}} \) and performing a sweep on \( n \) and \( R_L \), each of the curves represents a certain \( n \) ranging from 1 to the limit set by the outer diameter, and within each curve different \( w \) values starting from \( w = w_{\text{min}} \) up to the maximum value that can fit within \( d_{\text{out}} \) for the corresponding \( n \) is then calculated and plotted. From this illustration it can be seen that while increasing the number of turns increases the maximum achievable inductance it also increases the parasitic resistance which suggests that a trade-off can be found.
The second approach is shown Fig. [7.14] and it is achieved by solving the same three equations for $L$ and $n$ instead of $L$ and $w$ and plotting $L(R_L, w, s)$ where a sweep is executed on $w$ and $R_L$. Every curve represents a certain $w$ ranging from $w = w_{\text{min}}$ up to the maximum value that fits within $d_{\text{out}}$. Within a curve, each point represents a given $n$ from 1 up to the maximum set by the given area.

By examining the previous curves it can be seen that a trade-off envelope exists for a given area and frequency that would maximize the inductance time-constant ratio. The steps to finding the trade-off curve are as follows:

1. Solve the three main equations to get two equations; one for the inductance in the form $L(n, w, s)$, and the other is for the parasitic resistance in the form $R_L(n, w, s)$, thus eliminating $d_{\text{avg}}$.
2. Solve the resulting parasitic resistance equation for $w$ to get an expression of the form $w(R_L, n, s)$.
3. Substitute from $w(R, n, s)$ into the inductance equation to get an expression of the form $L(R_L, n, s)$.
4. Differentiate the resulting inductance with respect to the number of turns $\frac{\partial L(R_L, n, s)}{\partial n}$. 

Figure 7.13: Curves of all possible number of turns for an inductor of a given area with $k = 0.55$. 

$\begin{align*}
L & \quad 140 \\
\text{n increasing} & \quad 100 \\
\text{RL} & \quad 120 \\
& \quad 80 \\
& \quad 40 \\
\end{align*}$
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Figure 7.14: Curves of all possible widths for an inductor of a given area with \( k = 0.55 \).

5. Equate the derivative from the previous step to zero and solve for \( n \).

6. Substitute for \( n \) in \( L(R_L, n, s) \), where \( n \) is obtained as a value from the previous step.

7. Plot \( L(R_L) \), where \( L : L_{\text{min}} \Rightarrow L_{\text{max}} \) and \( R_L : R_{L_{\text{min}}} \Rightarrow R_{L_{\text{max}}} \) (The limits were obtained in the previous section).

**Algorithm 1** The \( L/R_L \) trade-off envelope.

1: Solve Eq. (4.3), (4.7), (4.9) simultaneously
2: Reduce to \( L(n, w, s_{\text{min}}) \) and \( R_L(n, w, s_{\text{min}}) \)
3: Solve \( R_L(n, w, s_{\text{min}}) \) for \( w \)
4: Substitute \( w(R_L, n, s_{\text{min}}) \) into \( L(n, w, s_{\text{min}}) \)
5: Solve \( \frac{\partial L(R_L, n, s_{\text{min}})}{\partial n} = 0 \) for \( n \)
6: Substitute \( n \) into \( L(n, w, s_{\text{min}}) \)
7: Plot \( L(R_L) \), where \( L : L_{\text{min}} \Rightarrow L_{\text{max}} \) and \( R_L : R_{L_{\text{min}}} \Rightarrow R_{L_{\text{max}}} \)

The resulting trade-off envelope for an inductor with \( k = 0.55 \), is depicted in Fig. 7.15. The envelope in solid black is appended to Fig. 7.13 and Fig. 7.14. As can be seen the envelope tracks
all the points where $L/R_L$ is maximized providing the achievable limit of $L/R_L$ for a given area and frequency.

The same algorithm can be applied to inductors with different values of $k$ occupying the same area. In order to compare different trade-off envelopes for different inductors, the same approach was performed on an inductor with $k = 0$ (square) and another one with $k = 1$ (regular octagon). Trade-off curves for three different inductors occupying an area of 0.25 mm$^2$ are shown in Fig. 7.16. The normalized resistance limit is chosen as 800 squares, since for most fabrication technologies this would correspond to a resistance limit of 4 to 8 Ω. As expected, the trade-off curve of the inductor with $k = 0.55$ in solid black has the highest inductance time-constant ratio, the inductor with $k = 1$ in dotted black follows, and the inductor with $k = 0$ in dashed black is the lowest.

### 7.3.2 Approximate optimization equation

An approximate equation that maximizes the inductance time constant ratio has been developed for each shape. The expression is of the form $L_{opt}(s, R)$, where $s$ is the normalized segment
Figure 7.16: The normalized inductance versus parasitic resistance for $k = 0.55$ (solid), $k = 1$ (dotted), and $k = 0$ (dashed).

Table 7.1: Coefficients for the $L/R_L$ optimization equation.

<table>
<thead>
<tr>
<th>$k$</th>
<th>$x_1$</th>
<th>$x_2$</th>
<th>$y_1$</th>
<th>$y_2$</th>
<th>$z_1$</th>
<th>$z_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.153</td>
<td>21.12</td>
<td>0.0371</td>
<td>0.448</td>
<td>4.839×10$^{-7}$</td>
<td>0.00069</td>
</tr>
<tr>
<td>0.55</td>
<td>0.247</td>
<td>23.86</td>
<td>0.0393</td>
<td>0.605</td>
<td>4.887×10$^{-7}$</td>
<td>0.00079</td>
</tr>
<tr>
<td>1</td>
<td>0.226</td>
<td>23.61</td>
<td>0.0373</td>
<td>0.534</td>
<td>4.676×10$^{-7}$</td>
<td>0.00074</td>
</tr>
</tbody>
</table>

where coefficients $x_1, x_2, y_1, y_2, z_1,$ and $z_2$ are shape-dependent constants given in Table 7.1. The inductance and resistance in the expression are both normalized. The expression can be used for inductors of different areas and frequencies. The area is embedded in the expression as a function of the normalized segment spacing, while the frequency is taken into consideration in the sheet resistance which gets multiplied by the normalized resistance to denormalize it. The inductance is multiplied by $d_{out} \times \mu_1 \times \mu_0$ for denormalization. The maximum error for this expression is below 3.2% for a minimum total inductor length of 800 squares.
7.4 Design examples

Three inductors were designed and simulated using ASITIC in the TSMC 65-nm technology. The inductors have \( k \) of 0, 0.55, and 1. All three inductors were implemented in the topmost metal layer (M9), which has a sheet resistance of about 6 m\( \Omega \)/\( \square \). Each inductor was enclosed in a rectangle of 0.25 mm\(^2\). The spacing between segments \( s \) for all three inductors was chosen as the minimum permitted by the technology (2 \( \mu \)m) in order to maximize the value of \( L/R_L \). The frequency of operation is chosen to be 100 MHz.

We start by employing the algorithm developed in the previous section by plotting the trade-off curve of all three inductors given the area and minimum spacing as shown in Fig. 7.16, in order to get the minimum value of \( R_L \) for a chosen inductance. The first inductor taken into consideration is the one with \( k = 0 \), an arbitrary normalized inductance of 7.8 is chosen which corresponds to a resistance of 234 squares. We then work the algorithm backwards in order to get the specification of the inductor, namely the segment width and the number of turns, so that it can be analyzed and designed in ASITIC. For finding \( n \), from step 6 of the algorithm, we solve \( L(R_L, n, s_{\text{min}}) \), with the given values of \( L \), \( R_L \), and the normalized \( s_{\text{min}} \), for \( n \) which results in \( n = 6 \). For finding \( w \), from step 3, we solve \( R_L(n, w, s_{\text{min}}) \) for \( w \), with the given values of \( R_L \), and \( s_{\text{min}} \), and the acquired value of \( n \), which results in a normalized width of 0.0595. Next, we denormalize the geometrical parameters by multiplying them by \( d_{\text{out}} \). In order to be able to compare all three inductors we repeat the same steps for the other two inductors, while fixing the value of the inductance, as expected, this will result in different values of resistance and segment width. Since the inductors have the same area and inductance the number of turns will not change for this case. The resulting specifications for the three inductors are as follows: for the inductor
with $k = 0$, $w$ is 29.77 $\mu$m, $s$ is 2 $\mu$m, and $n$ is 6, for the inductor with $k = 0.55$, $w$ is 28.75 $\mu$m, $s$ is 2 $\mu$m, and $n$ is 6, and for the inductor with $k = 1$, $w$ is 26.65 $\mu$m, $s$ is 2 $\mu$m, and $n$ is 6. The three inductors are shown in Fig. 7.17. The denormalized value of inductance for all three inductors is about 11.49 nH. The denormalized values of the resistance are as follows: for $k = 0$, 1.56 $\Omega$, for $k = 0.55$, 1.48 $\Omega$, and for $k = 1$, 1.53 $\Omega$.

The three inductors are then designed and simulated in ASITIC to compare the obtained results of $L$ and $R_L$ with those of the algorithm. The simulated inductor with $k = 0$, has an inductance of $L = 11.57$ nH and a resistance of $R_L = 1.6$. The simulated inductor with $k = 0.55$, has an inductance of $L = 11.56$ nH and a resistance of $R_L = 1.51$. The simulated inductor with $k = 1$, has an inductance of $L = 11.55$ nH and a resistance of $R_L = 1.56$. The maximum error in inductance between the algorithm and ASITIC is 0.7%, while the maximum error in resistance between the algorithm and ASITIC is 2.6%.

### 7.4.1 Boost converter example

Three identical boost converters, one for each inductor (Fig. 7.18), were also designed and simulated. The switching frequency is 100 MHz, and the filter capacitance is 200 pF. The transistors used are high-voltage devices rated for 2.5 V operation. The switches occupy an area of about 0.014 mm$^2$. The converters are operated in an open-loop fashion, since the choice of a control scheme is irrelevant to the comparison. The input voltage $V_{IN}$ is kept constant at 1 V.

In the first simulation, the output voltage, $V_{OUT}$, is kept constant at 2 V. Load currents ranging from 2 mA to 25 mA for an output power range of 4 mW to 50 mW were simulated. The inductor with $k = 0$ is represented by a dashed curve, while the inductor with $k = 0.55$ is in solid black, and the inductor with $k = 1$ is represented by a dotted curve as shown in Fig. 7.19. As expected,
the conversion efficiency of the converter with the inductor with $k = 0.55$ is highest throughout the whole range, followed by the one with $k = 1$, while the lowest being the one with $k = 0$. The maximum improvement achieved is about four percentage points.

In the second simulation, $I_{OUT}$ was kept constant at 10 mA, while $V_{OUT}$ was swept from 1.1 V to 2.4 V. As shown in Fig. 7.20, the conversion efficiency of the converter with the $k = 0.55$ inductor exceeds the other two converters by a maximum of about three percentage points. This improvement is in line with the analysis shown in Fig. 7.1 and it was obtained for the same silicon area and with no other modifications to the converter design.

7.4.2 Buck converter example

Similarly, three identical buck converters, one for each inductor (Fig. 7.21), were also designed and simulated. The switching frequency is 100 MHz, and the filter capacitance is 500 pF. The transistors used are standard TSMC 65-nm devices rated for 1 V operation. The switches occupy an area of about 150 $\mu$m². The converters are operated in an open-loop fashion, since the choice of a control scheme is irrelevant to the comparison. The input voltage $V_{IN}$ is kept constant at 1 V.

In the first simulation, the output voltage, $V_{OUT}$, is kept constant at 0.5 V. Load currents
Figure 7.20: Conversion efficiency versus voltage gain for $I_{OUT} = 10$ mA, for inductors with $k = 0$ (dashed), $k = 0.55$ (solid), and $k = 1$ (dotted).

Figure 7.21: Schematic of the buck converter used for the design example.
Figure 7.22: Conversion efficiency versus load current for $V_{OUT}/V_{IN} = 0.5$, for inductors with $k = 0$ (dashed), $k = 0.55$ (solid), and $k = 1$ (dotted).

Figure 7.23: Conversion efficiency versus voltage gain for $I_{OUT} = 10$ mA, for inductors with $k = 0$ (dashed), $k = 0.55$ (solid), and $k = 1$ (dotted).
ranging from 5 mA to 60 mA for an output power range of 2.5 mW to 30 mW were simulated. The inductor with \( k = 0 \) is presented by a dashed curve, while the inductor with \( k = 0.55 \) is in solid black, and the inductor with \( k = 1 \) is presented by a dotted curve as shown in Fig. 7.22. As expected, the conversion efficiency of the converter with the inductor with \( k = 0.55 \) is highest throughout the whole range, followed by the one with \( k = 1 \), while the lowest being the one with \( k = 0 \). The maximum improvement achieved is about three percentage points.

In the second simulation, \( I_{\text{OUT}} \) was kept constant at 10 mA, while \( V_{\text{OUT}} \) was swept from 0.3 V to 0.8 V. As shown in Fig. 7.23, the conversion efficiency of the converter with the \( k = 0.55 \) inductor exceeds the other two converters by a maximum of about two percentage points.

### 7.5 Summary

In this chapter, the relationship between the conversion efficiency and the inductance time-constant ratio was analyzed to show the importance of optimizing this ratio. In the second section the geometrical parameters were studied to see how changing each parameter affects the \( L/R_L \) ratio. A shape factor \( k \) was introduced to describe different inductor shapes and then optimized for maximizing the \( L/R_L \) ratio. The trade-off algorithm was developed in the third section. The fourth section provided two design examples, one for the boost converter and one for the buck, to compare the performance of three inductors with different \( k \) factors.
Chapter 8

Design considerations

This chapter discusses the design considerations of the boost converter. Since fully integrated boost converters suffer from lower conversion efficiencies. Different design approaches were implemented here in order to optimize the efficiency further.

All designs used TSMC 65-nm technology (CMN65GP). This technology offers a top thick metal layer (M9) that is made of copper with a sheet resistance of about 6 mΩ/□. In Section 8.1 the multiple topologies considered for the chip design are discussed along with the pros and cons of each. In Section 8.2 the pulse-width-modulation and pulse-frequency-modulation schemes are discussed.

8.1 Boost converter design considerations

Many approaches were considered during the design process to make the best use of the given inductor area, two of which will be considered in detail in the next two subsections.

8.1.1 Single inductor vs. coupled inductors

The first approach was to consider and compare two converters, one based on a single inductor occupying a certain area and another one based on coupled inductors implemented in the same area in two metal layers stacked on top of one another.

Coupled inductors have been widely used since their introduction [96]. One of the significant advantages they provide is that the ripple of one inductor could be shifted to the other
inductor, thus achieving an almost ripple-free current in the first inductor. They also allow for increasing the energy density without increasing the component count [79]. Additionally, in some applications, a low ripple input current is desirable to meet the relevant Electromagnetic Interference (EMI) requirements, and minimize the total harmonic distortion. Previous papers discussed replacing the inductor of a boost converter with coupled inductors [77, 80]. However, those implementations target discrete inductors, and are not readily applicable to fully integrated converters. An implementation that uses integrated coupled inductors for boost converters was reported [97], however, it does not provide an analytical model that can be used to compare the conversion efficiency to that of the single-inductor converter.

Since integrated dc-dc converters in CMOS technology tend to have small values of inductance (few tens of nH), because of the limited available area. This leads to high switching frequencies and in most cases to discontinuous conduction mode (DCM). Since in DCM the current through the inductor \(i_L(t)\) varies between a positive value and zero, further input-current harmonics and EMI are introduced, which the coupled configuration might help mitigate. In the boost converter shown in Fig. 8.1, assuming at first that the inductors be ideal (i.e. \(R_p = R_s = 0\)), the change in current through the primary and secondary inductors (\(i_{Lp}\) and \(i_{Ls}\)) would be

\[
\frac{di_{Lp}}{dt} = \frac{V_{Lp}L_s - V_{Ls}L_m}{L_p L_s (1 - k^2)} , \quad \frac{di_{Ls}}{dt} = \frac{V_{Ls}L_p - V_{Lp}L_m}{L_p L_s (1 - k^2)} ,
\]

(8.1)

where \(L_m\) is the mutual inductance given by

\[
L_m = k\sqrt{L_p L_s}.
\]

(8.2)

One of the main advantages of this configuration is the ability to steer the current through the secondary inductor to get a ripple free current in the primary inductor, which requires \(k\) to be \(\sqrt{L_s/L_p}\). It can be assumed that the capacitor \(C_S\) is large enough that \(V_{Lp} \approx V_{Ls}\).
The inclusion of the resistances, $R_{Lp}$ and $R_{Ls}$, increases the ripple current in the primary inductor. Parasitic resistances in discrete inductors can be negligible [79], but they are a major loss contributor in integrated inductors. The average current through the secondary inductor in steady state will still be zero due to the series-connected capacitor $C_S$. However, the ratio of ripple current between primary and secondary inductor will be highly dependent on the ratio of the resistances.

The energy dissipated over a resistor in a single clock cycle for a single inductor is a function of the current through the inductor, the period, and the inductor resistance

$$E_{RL} = \int_0^T i_L(t)^2 R_L dt. \tag{8.3}$$

Solving the integral yields the energy dissipated by a single inductor in DCM. For the coupled inductors, the integral is divided into two intervals and the total energy dissipation is

$$E_{RLt} = \int_0^{\sqrt{\alpha}} i_L(t)^2 R_L dt + \int_{\sqrt{\alpha}}^T i_L(t)^2 R_L dt$$

$$= \frac{T V_{OUT}^4}{3 R^2 V_{IN}^2} \left( R_{Lp} (3(1 - \gamma) + 4 \gamma^2 \sqrt{\alpha}) + R_{Ls} (4(1 - \gamma)^2 \sqrt{\alpha}) \right), \tag{8.4}$$

where $\gamma$ is the ratio between the ripple current in the primary inductor to the sum of the ripple in the primary and secondary inductors

$$\gamma = \frac{\Delta I_{Lp}}{\Delta I_{Lp} + \Delta I_{Ls}}. \tag{8.5}$$

By comparing $E_{RL}/E_{RLt}$ we get a ratio for the change in efficiency between the single-inductor converter and the coupled-inductor one

$$\frac{\eta_s}{\eta_c} = \frac{4 R_L \sqrt{\alpha}}{R_{Lp} \left( 3 \gamma^2 - 1 + 4 \gamma^2 \sqrt{\alpha} \right) + R_{Ls} (1 - \gamma)^2 \left( 4 \sqrt{\alpha} - 3 \right)}. \tag{8.6}$$

The parasitic capacitances of the integrated inductor can be appended to the model without increasing the complexity as the main impact would be to the current drawn by the converter

$$\Delta I_{OUT} = V_{OUT} C_{EQ} f_{SW}. \tag{8.7}$$
The change in $I_{OUT}$ can then be used to approximate the new efficiency of the converter.

Another approach that was also designed is a boost converter with two coupled inductors in parallel is shown in Fig. 8.2. These inductors are implemented as two identical spirals on adjacent metal layers (in this paper the top layer, M9, and the second top layer, M8), therefore achieving a coupling coefficient above 98%. This configuration does not increase the inductance value, but it decreases the parasitic resistance of the equivalent inductor. The equivalent inductance is determined using the coupling coefficient $k$

$$L_{EQ} = \frac{L_p(1 - k^2)}{2(1 - k)}. \quad (8.8)$$

The equivalent parasitic resistance

$$R_{EQ} = \left(\frac{1}{R_{LP}} + \frac{1}{R_{LS}}\right)^{-1}, \quad (8.9)$$

is lower than the initial parasitic resistance and results in a decrease in the energy lost over the inductors. The analysis of the single inductor converter can be readily applied to the parallel coupled inductors converter by replacing $L$ and $R_L$ by $L_{EQ}$ and $R_{EQ}$.

Both configuration along with a conventional single-inductor converter were designed and simulated in the TSMC 65-nm technology in Cadence at 100 MHz [98]. The inductors were first optimized for the chosen area and frequency [99], and then designed and simulated in ASITIC [36], in order to extract the parasitics to be used in Cadence. Each inductor occupied an area of 0.25 mm$^2$. For all simulations the input voltage is 1 V. For the single inductor simulations, the inductor is implemented in M9 which is a copper layer with a thickness of 3.4 $\mu$m. Fig. 8.3 shows a comparison between our analytical model and the simulations. The output voltage,
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Figure 8.3: The load current versus conversion efficiency for \( V_{IN} = 1 \) V, \( V_{OUT} = 2 \) V, \( f_{SW} = 100 \) MHz, \( L = 15 \) nH, \( R_L = 2.26 \) \( \Omega \), \( C_L = 765 \) fF.

\( V_{OUT} \), is 2 V, the inductance, \( L \), is 15 nH, the parasitic resistance, \( R_L \), is 2.26 \( \Omega \), the total parasitic capacitance \( C_L \) is 765 fF. A parametric sweep on output current from 0.5 mA to 4 mA was performed and Fig. 8.3 shows that the maximum error percentage between the analytic model and simulations is 2.2%. Since the parallel coupled-inductor converter uses the same analysis as the single inductor with modifying \( L \) and \( R_L \), the simulations and analysis show the same trend as the single inductor converter.

The coupled-inductor converter simulations for load currents of 0.5 mA to 4 mA are shown in Fig. 8.4. The primary inductor is identical to the single inductor, however; the secondary inductor is implemented in M8, which is an aluminium layer with a thickness of 0.9 \( \mu \text{m} \). This in turn introduces larger parasitic resistance and capacitance since M8 is closer to the substrate. Shunting metal layers 8 and 7 to form a single secondary inductor has been previously reported [6], in our case it provides a decrease of 13.5% in the parasitic resistance, however, it increases the equivalent capacitance by 27.9%. This is due to the fact that the thickness of M7 is four times less than M8 and is closer to the substrate. Therefore, the reduction in parasitic resistance does not compensate for the increase in capacitance, and hence it is better to use only M8 for the secondary inductor. The parasitic resistance of the secondary inductor, \( R_{Ls} \) is 7.35 \( \Omega \) and the equivalent parasitic capacitance is 1.1 pF. Since the two inductors are identical in size and implemented on top of each other, the coupling coefficient, \( k \), is 98.7%. The maximum error between the proposed analytical model and simulations is below 2%. 
Additionally, all three configurations were simulated for output voltages ranging between 1.2 and 2.5 V, since 2.5 V is the maximum voltage allowed by the technology. The load current is kept at 2 mA, and all other conditions are the same. As it is shown in Fig. 8.5, all three configurations show very close performance with the maximum efficiency decrease between the coupled and the single inductor converters being below 3%. The main advantage of the coupled-inductor converter over the conventional single inductor converter is highlighted in Fig. 8.6. The current ripple of the inductor of the conventional converter is represented by the solid black curve, while the current of the primary inductor of the coupled-inductor converter is represented by the dashed grey curve. As expected, the coupled-inductor converter shows a ripple reduction of 24.5%.

Based on this discussion, the chosen configuration was the single-inductor converter, as the reduction in ripple inductor current was not significant enough to justify the added area for implementing the capacitor $C_S$ which needs to be large in order for $V_{LP} \approx V_{LS}$.

### 8.1.2 Single inductor vs. dual inductors

The second approach given a certain area for an inductor is to figure out whether to implement a single inductor or multiple inductors where each carries the single inductor current divided by the number of inductors $n$. Based on the discussion in the previous chapter, the family of curves
Figure 8.5: The conversion ratio versus conversion efficiency for $V_{IN} = 1$ V, $V_{OUT} = 2$ V, $f_{SW} = 100$ MHz, $L_p = L_s = 15$ nH, $R_{lp} = 2.26 \Omega$, $R_{ls} \approx 7.4 \Omega$, $C_L = 1.1$ pF, $k = 0.98$.

Figure 8.6: Current ripple in the single-inductor converter (solid), and in the primary of the coupled-inductor converter (dashed).
in the parameter $n$

$$L(n, R_L) = \frac{\mu_0 \mu_1 d_{out} n^2 \left( \frac{R_L}{R_{\Box}} + 2n \right)^2}{\left( \frac{R_L}{R_{\Box}} + 4n^2 + 2n \right) \left( \frac{R_L}{R_{\Box}} + 4n^2 \mu_2 + 2n \right)}$$  \hspace{1cm} (8.10)$$

where $\mu_0$, $\mu_1$, $\mu_2$, $R_{\Box}$, and $d_{out}$ are constant.

Observing that $R_L/R_{\Box} \gg 2n$ for geometrical reasons, (8.10) can be approximated as

$$L_s(n, R_L) = \frac{\mu_0 \mu_1 d_{out} n^2 \left( \frac{R_L}{R_{\Box}} \right)^2}{\left( \frac{R_L}{R_{\Box}} + 4n^2 \right) \left( \frac{R_L}{R_{\Box}} + 4n^2 \mu_2 \right)}.$$  \hspace{1cm} (8.11)$$

The envelope of $L_s(n, R_L)$ is then derived by setting

$$\frac{\partial L_s(n, R_L)}{\partial n} = 0,$$  \hspace{1cm} (8.12)$$

eliminating $n$ from (8.11), and obtaining

$$L_{env} = \frac{\mu_0 \mu_1 d_{out}}{4 \left( \sqrt{\mu_2 + 1} \right)^2} R_L,$$  \hspace{1cm} (8.13)$$

which gives the highest $L$ for any given $R_L$.

We start by designing a dual-inductor converter as shown in Fig. 8.7. Since fully integrated boost converters tend to operate in DCM due to the sizes of the inductors, the operation of the converter is explained in DCM. The dual-inductor converter consists of two identical inductors, $L_2$, each of which occupies half the area and has half the value of $L_1$, and the two corresponding parasitic resistances $R_{L2}$. The converter uses the same input voltage $V_{IN}$, filter capacitor $C$, and load resistor $R$. The switching network of the converter consists of two identical NMOS switches, $M_{n2a}$ and $M_{n2b}$, and two identical PMOS switches, $M_{p2a}$ and $M_{p2b}$, which are half the size of the corresponding transistors in the single-inductor converter. The two phase signals $\phi_{1a}$ and $\phi_{2a}$ are in antiphase with $\phi_{1b}$ and $\phi_{2b}$.

At $t = 0$, $\phi_{1a}$ and $\phi_{2a}$ are high setting $M_{n2a}$ on and $M_{p2a}$ off until $t = DT$. In the second phase, $M_{n2a}$ is off and $M_{p2a}$ on until $t = (D + D_1)T$, when eventually both $M_{n2a}$ and $M_{p2a}$ turn off until the next cycle. At $t = T/2$, $\phi_{1b}$ and $\phi_{2b}$ turn high setting $M_{n2b}$ on and $M_{p2b}$ off until $t = (1/2 + D)T$. At this point, $M_{n2b}$ is off and $M_{p2b}$ on until $t = (1/2 + D + D_1)T$, when both
$M_{n2b}$ and $M_{p2b}$ turn off until the next cycle. The different phases are shown in Fig. 8.8. The dual-inductor and the single-inductor converters transfer the same average power to the load. However, since in the dual-inductor converter the energy is delivered to the load in two steps per period, the output voltage ripple is reduced.

Dividing the original converter in $n$ equal parts, the area and the value of the inductance is divided by $n$ in each part (i.e. $L_n = L_1/n$) and the average current provided to the output by each part is divided by $n$ (i.e. $I_{OUTn} = I_{OUT}/n$). As an example, for the conventional converter with a single inductor $n = 1$, and for the dual-inductor converter $n = 2$, and so on. At the same time, the areas of the switches are divided by $n$ resulting in on resistances multiplied by $n$, while $V_{IN}$ and $V_{OUT}$ are assumed to be constant. The efficiency of the $n$-inductor converter is found to be

\[ \eta_n = \frac{1}{1 - \frac{R_{CL}}{V_{OUT}} + \frac{I_{OUT}}{V_{IN}} \left( R_L + n \left( R_{on1} + \frac{V_{IN}R_C}{V_{OUT}} \right) \right) \sqrt{\frac{8(V_{OUT} - V_{IN})}{9L_1f_I}}}. \]  

(8.14)

Taking the differential of the efficiency with respect to $n$, results in the condition at which the efficiency of the converter with $n$ inductors is higher than the efficiency of the converter with $n - 1$ inductors

\[- \frac{d R_{Ln}}{dn} > R_{on1} , \]

(8.15)
which using (8.13) in the case of single and dual inductors corresponds to

\[
R_{L1} - R_{L2} = \frac{2(\sqrt{K_2} + 1)^2 R_{\square} L_1}{\mu_0 K_1 d_{out}} > R_{on1}.
\]  

(8.16)

In this condition the dual-inductor converter has a higher efficiency than the single-inductor converter.

A single-inductor converter was designed in addition to the dual-inductor one [100]. The area occupied by the inductance of the single-inductor converter is a square of 500 μm by 500 μm, which is equal to the total area occupied by both inductors of the dual-inductor converter. All inductors were implemented in the topmost metal layer (M9). The single inductor, \(L_1\), was optimized for an inductance of 15 nH which corresponds to a parasitic resistance, \(R_{L1}\), of 2.05 Ω. Each of \(L_2\) has an inductance of 7.5 nH and a parasitic resistance, \(R_{L2}\), of 1.45 Ω, which results in a change in resistance \(R_{L1} - R_{L2} = 0.60\) Ω. Both converters have an input voltage, \(V_{IN}\), of 1 V and an output voltage, \(V_{OUT}\), of 2 V. The average load current in both converters is 9 mA, which results in an output power of 18 mW. The switching frequency, \(f\), is 100 MHz, and the filter capacitance in both converters is 200 pF.

For the simulations, the sizes of the NMOS and the PMOS of the single-inductor converter were chosen to achieve a range of on resistances, \(R_{on1}\), from 0.2 Ω to 3 Ω. The sizes of the two NMOS transistors of the dual-inductor converter were chosen to be half the size to result in a range of on resistances, \(R_{on2}\), from 0.4 Ω to 6 Ω. The conversion efficiency of both converters was calculated from the simulation results. As can be seen from Fig. 8.9 at an on resistance of 0.2 Ω, the efficiency of the dual-inductor converter is almost 85% while the efficiency of the single-inductor is 80.7%. For the considered parameters the condition in (8.16) is \(R_{on1} < 0.86\) Ω.
and, as expected by the analysis, when the on resistance is around this value, the efficiencies of both converters are almost the same. As the on resistance increases further both efficiencies drop, however, the efficiency of the dual-inductor converter drops faster. Therefore, for high on resistances, a single-inductor converter is the converter of choice.

The dual-inductor converter can provide lower output voltage ripple. As the simulations show in Fig. 8.10, the ripple voltage of the single-inductor converter in grey is about 383 mV, and the ripple of the dual-inductor converter in black is about 190.8 mV, a decrease of about 50% as expected. Since the chip area is a tight constraint, the capacitor size can be decreased by half, while maintaining the same amount of ripple as in the single-inductor converter. Alternatively, the same capacitor can be used to cut the ripple in half without any area penalty.

### 8.2 Control schemes

The two main methods of controlling dc-dc converters are pulse width modulation (PWM) and pulse frequency modulation (PFM) [21]. PWM is popular in standard dc-dc converters, due to its robust ability to handle different output voltages and load currents. PWM operates by keeping the time period constant and varying the duty cycle of the charging phase of the converter. PFM operates by keeping the duty cycle constant and varying the frequency of the delivered charge.
and discharge phases [5]. Some complex designs even combine both controls [101].

The factors influencing the choice of the control systems of integrated dc-dc converters are different from those of traditional discrete-component dc-dc converters. Therefore, this section examines and compares integrated step-up dc-dc converters controlled using PWM and PFM.

The PWM control functions by changing the width of the duty cycle (the inductor’s charging time interval) for a given switching frequency [102, 103]. A PWM control can be voltage mode [104] or current-mode [105–107]. It can also be feedforward [108] or feedback [104]. As the duty cycle gets larger, the amount of current delivered to the load at a constant $V_{IN}$ and $V_{OUT}$ gets higher as shown in Fig. 8.11.

The block diagram of a PWM controlled converter can be seen in Fig. 8.12 [109]. The main concept of generating a PWM signal is comparing a triangular waveform with a constant frequency $f_{SW}$ to produce an error voltage $v_E$. The error voltage is obtained by comparing the output voltage to a reference voltage $V_{REF}$. If $v_E$ has a larger amplitude than the triangular waveform, then the output of the comparison is a logic high and vice versa. This output drives the NMOS switch and gets passed through the logic that drives the PMOS switch. The duty cycle is proportional to the amplitude of $v_E$ [5, 110].

The PFM control functions by varying the frequency of the pulses while keeping the duty cycle constant, where increasing the load current involves increasing the frequency of the pulses as shown in Fig. 8.13 [109]. The control works by charging and discharging the inductor in the event that the output voltage falls below a certain threshold. The block diagram of a PFM

![Figure 8.10: The output voltage ripple of the dual-inductor converter (black) and the single-inductor converter (grey).](image)
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Figure 8.11: PWM waveforms.

Figure 8.12: Block diagram of a PWM controlled converter.
controlled converter can be seen in Fig. 8.14. There are two comparators in the circuit, the first one is used to test for when the load voltage falls below the desired $V_{OUT}$, which triggers the start of phase 1. The second comparator is used to control the PMOS in the same fashion as in the PWM control.

Figs. 8.11 and 8.13 illustrate the differing load currents in the two control systems, where $I_{OUT1}$ is a given load current in the DCM range, $I_{OUT2}$ is double $I_{OUT1}$, and $I_{OUT3}$ is double $I_{OUT2}$. Given that PFM has a constant pulse width, the energy delivered per pulse will be constant, this means that the switching frequency is directly proportional to $I_{OUT}$. For PWM the energy delivered per pulse is proportional to the square of the pulse width, meaning $T_1$ is proportional to $\sqrt{I_{OUT}}$.

As an illustration, an optimization curve that relates $T_1$ to the conversion efficiency is shown in Fig. 8.15. As $T_1$ increases, the resistive losses dominate, however, if the pulse width decreases too much, the capacitive losses dominate. The implications of this are that the efficiency varies
substantially with load current in PWM systems, as the value of $T_1$ changes with load current.

Both control systems along with the boost converter were designed and simulated in the TSMC 65-nm technology (CMN65GP). The inductor was designed and simulated using ASITIC [36]. The inductor is implemented in the topmost layer (M9) and occupies an area of $450 \times 450 \mu\text{m}^2$. The inductance value is 8.05 nH, the average parasitic resistance value is 1.22 $\Omega$, and the parasitic capacitance is 552 fF. All the simulations are performed with an input voltage $V_{IN}$ of 1 V. The converter uses high voltage MOSFETs that are rated for 2.5 V. The frequency of the PWM controlled converter is kept constant at 100 MHz, while the frequency of the PFM controlled is ranging from 20 to 150 MHz.

**Conversion efficiency vs. load current**

Simulations were performed to determine the relationship between the conversion efficiency of both control schemes at different load currents. The output voltage $V_{OUT}$ was held constant at 2 V. The same boost converter circuit was simulated using both PFM and PWM control schemes. Load currents varying from 1 to 12 mA were simulated. The result of the simulation of the PFM controlled converter is shown in Fig. [8.16], where the model is shown in solid black and the simulation results are shown in dashed black. The simulation of the PWM controlled converter is shown in Fig. [8.17].

The results of the simulations agree with the analysis for both the PWM and PFM control methods. The efficiency of the PFM remains relatively constant across varying load currents,
Figure 8.16: The conversion efficiency versus load current for a PFM controlled converter with a constant output voltage of 2 V.

Figure 8.17: The conversion efficiency versus load current for a PWM controlled converter with a constant output voltage of 2 V.
while there is larger variation in the efficiency of the PWM with respect to load currents. The PFM is capable of retaining higher efficiency, especially at lower load currents as the converter can be better optimized for the specific pulse width that is chosen. At medium to higher load currents, the PWM should outperform the PFM system.

Conversion efficiency vs. output voltage

Simulations were performed to demonstrate the relationship between the efficiency and the output voltage. The load current was held constant at 6 mA, and the output voltage was swept on from 1.2 to 2.4 V while the input voltage was kept at 1 V. The simulations were performed using both the PFM (Fig. 8.18) and PWM (Fig. 8.19) control, and the simulation results were again compared to the values from the analysis.

The difference between the simulation results and the analysis when sweeping on the output voltage is largely due to the non-linear effects of the transistor parasitics (not considered in the model) and how they influence the conversion efficiency.
Lastly, the ability of both control systems to regulate the output voltage under the varying load conditions was simulated. For both PFM Fig. 8.20 and PWM Fig. 8.21, the load current was stepped from 1 to 8 mA with a frequency of 5 MHz.

The PFM control is more effective at providing a stable output voltage in the presence of changing load currents, especially at low load currents. The PWM controlled converter, on the other hand, showed higher performance at higher load currents. Since the interest of this work is higher loads ($P_{OUT} > 5$ mW), PWM is the chosen control scheme of choice. It should be noted that at low loads ($P_{OUT} < 10$ mW) monolithic charge pump dc-dc step-up converters are a better choice in terms of area and conversion efficiency [5].

8.3 Summary

In this chapter, different design topologies for boost converters were designed with example implementations to show the reasoning behind the choices made for the test chip design. Different control schemes were also discussed.
Figure 8.20: The conversion efficiency versus output voltage for a PFM controlled converter with a constant load current of 6 mA.

Figure 8.21: The conversion efficiency versus output voltage for a PWM controlled converter with a constant load current of 6 mA.
Chapter 9

Test chip design and simulations

In this chapter, the details of the test chip design are presented. Section 9.1 discusses the design process of all the blocks of both the boost and buck converters in detail. The circuit simulations of the boost converters are included in Section 9.2 while the buck converter circuit simulations are included in Section 9.3. The results are discussed in Section 9.4.

9.1 Test chip design

9.1.1 Fabrication technology

The test chip is designed in a TSMC 65-nm (CMN65GP) CMOS process (nominal supply voltages are 1 and 2.5 V), with one polysilicon and 9 metal layers with the topmost layer made of copper with resistivity of about 6 mΩ/□. The technology also offers a triple well option and a MIM capacitor layer between metals 7 and 8. The technology offers a thick oxide layer which increases the breakdown voltage limit of the transistors making this technology suitable for the design. The core area of the design in 1.2 mm × 1.2 mm = 1.44 mm², and the total area including bonding pads is 1.5 mm × 1.414 mm = 2.121 mm². The devices used in the design of the test chip are reported in Table 9.1. The chip contains four converters, two of which are boost converters and two buck converters. Four inductors were implemented, two square-shaped inductors and two chamfered inductors. The specifications of the designed inductors are reported in Table 9.2. The layout of the overall test chip is shown in Fig. 9.1 where the upper two inductors are for the boost converters and the lower two are for the buck converter. The microscope photograph of the overall chip is shown in Fig. 9.2.
Table 9.1: Devices used from the TSMC 65-nm library.

<table>
<thead>
<tr>
<th>Device name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>nch</td>
<td>1 V standard VT NMOS transistor</td>
</tr>
<tr>
<td>pch</td>
<td>1 V standard VT PMOS transistor</td>
</tr>
<tr>
<td>nmos_rf_25</td>
<td>2.5 V NMOS transistor</td>
</tr>
<tr>
<td>pmos_rf_25</td>
<td>2.5 V PMOS transistor</td>
</tr>
<tr>
<td>mimcap</td>
<td>Base band MIM capacitor</td>
</tr>
<tr>
<td>nmoscap</td>
<td>NMOS in N-Well capacitor</td>
</tr>
<tr>
<td>rppolywo</td>
<td>P+ polysilicon resistor without salicide</td>
</tr>
</tbody>
</table>

Figure 9.1: Layout of the overall chip.
Figure 9.2: Microscope photograph of the overall test chip.
Figure 9.3: Layout of the inductors used in the design.
9.1.2 Tools and design flow

The design process started with mathematical functional verification using Mathematica. Behavioural-level design and simulations were created using MATLAB/Simulink along with VerilogA. Circuit-level design using the electronic design automation tool Cadence Composer and the circuit simulator Spectre was then performed to simulate and optimize the design. The design process is iterative, therefore multiple design-simulation cycles were carried out at this point to optimize the parameters and values of different components. The chip layout was drafted using the layout editing tool Cadence Virtuoso, while the Mentor Graphics tool Calibre was used for physical verification. The Design Rule Check (DRC) is performed using Calibre DRC for every block to avoid violations against design rules. The Layout Versus Schematic (LVS) is conducted using Calibre LVS to ensure that the netlists created from schematics of every block matches the netlists generated from the layout. The parasitics are extracted using Calibre Parasitic Extraction (PEX) to assess the parasitic elements of the layout and use them for simulations. The analog design flow [111] was followed to ensure correct functioning of the chip.

9.1.3 Boost converter circuit design

As mentioned previously, one of the two boost converters has a square inductor (Fig. 9.3(a)), while the other has a chamfered inductor (Fig. 9.3(b)). The schematic of the boost converter
Table 9.2: Inductors specifications.

<table>
<thead>
<tr>
<th></th>
<th>$L_1$</th>
<th>$L_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shape</td>
<td>square</td>
<td>chamfered</td>
</tr>
<tr>
<td>Size [$\mu$m]</td>
<td>$443 \times 459$</td>
<td>$457 \times 473$</td>
</tr>
<tr>
<td>Width [$\mu$m]</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>Spacing [$\mu$m]</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Number of turns</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>$k$</td>
<td>0</td>
<td>0.35</td>
</tr>
<tr>
<td>Inductance [nH]</td>
<td>8.05</td>
<td>8.22</td>
</tr>
<tr>
<td>Resistance [$\Omega$]</td>
<td>1.34</td>
<td>1.12</td>
</tr>
</tbody>
</table>

along with the PWM control block is shown in Fig. 9.4. The filter capacitor used is an NMOS capacitor with size $300 \ \mu m \times 200 \ \mu m$ and capacitance of 60 pF. Both switches are high voltage MOSFETs rated for 2.5 V (nmos$_{rf,25}$, pmos$_{rf,25}$) from Table 9.1. Both switches have a width of 5120 $\mu m$ and the feature length 0.28 $\mu m$. The switches are controlled by the phases $\phi_1$ and $\phi_2$ from the control block. The gate of $M_1$ is switched between $V_{IN}$ and ground. The gate of $M_2$ is switched between $V_{OUT}$ and $V_{IN}$. The bulk terminal of $M_2$ is connected to the output terminal, allowing the body diode to pass the inductor current between the charge and discharge phases. An input decouple capacitor was not implemented in order to make use of the additional inductance of the bondwire to be used for bonding the pad to the package’s pin. The converter is self-starting through the bulk connection of $M_2$.

The control block takes in three input signals from off the chip, $V_{REF}$ for the reference voltage, $CLKREF$ which is a voltage signal to tune the frequency of the on-chip oscillator, and $CLKAUX$ which allows for feeding in an external clock signal. The inductors for both converters are custom designed with the specifications reported in Table 9.2.

9.1.4 Boost control circuit design

The PWM control circuit diagram is reported in Fig. 9.5. This DCM PWM control system was designed and implemented occupying an area of about $150 \ \mu m \times 300 \ \mu m$. The operation is explained by means of its 5 sub-blocks as follows.
Figure 9.5: The block diagram of the PWM control system of the boost converter.
PWM block

This block generates a signal that controls the switches based on the output voltage level. The output voltage $v_{OUT}$ is first applied to the resistive divider formed by $R_1$ and $R_2$. The resulting fraction of the output voltage is then applied to a type-II compensator along with a reference voltage $V_{REF}$ that is fed from off-chip and is used to set the desired output voltage level. The compensator consists of an operational amplifier with negative feedback through $C_{f1}$, $C_{f2}$, and $R_f$. The output of the operational amplifier $v_{Er}$ is then applied to a comparator along with a triangular waveform that is produced by a ramp generator. The output of the comparator yields a PWM signal that can be directly fed to the NMOS drivers. The PWM signal also drives the current sensing block as will be shown next.

The operational amplifier is a folded cascode operational transconductance amplifier. The dc-gain is 54 dB, the bandwidth is 3 MHz, and the gain bandwidth product is 970 MHz. These values were chosen to ensure stable operation with the feedback for the output power range of the converter. The comparators are cross-coupled with positive feedback to ensure fast clipping and fast response [112].

Clock generation block

An on-chip oscillator is designed to generate a clock signal at 100 MHz. The clock generation block allows for choosing between the on-chip oscillator output or an external clock signal to pass to the ramp generator. The frequency of the oscillator can be tuned using the signal $CLKREF$. The same signal also feeds a high skewed inverter whose output is the selection pin of a multiplexer. When $CLKREF$ is below 800 mV the multiplexer selects the output of the oscillator to pass to the ramp generator. When $CLKREF$ rises above 800 mV the multiplexer passes the other input, $CLKAUX$ which is an external clock, to the ramp generator.

Current sensing block

Since this control system is designed for DCM control, the signal that is fed to the NMOS cannot be readily applied to the PMOS as in CCM. Additionally, the current through the PMOS needs to be measured in order for the PMOS to be turned off when the current reaches zero. This is achieved by measuring the difference between a fraction of the voltages at the drain and source of the PMOS, namely, $v_{SW}$ and $v_{OUT}$ through a second comparator. The values of the resistive divider formed by $R_3$, $R_4$, $R_5$, and $R_6$ are chosen such that the comparator changes state when the current through the PMOS is slightly positive to compensate for the delays of the comparator.
and the drivers. The block works as follows, when the signal of the NMOS driver goes high (the
NMOS is turned on at this point), the current sensing block is over-ruled and the output of the OR
gate goes high turning the PMOS off. The same signal is passed through a time delay block and
is fed to an inverter, after this time is over the current sensing is enabled which confirms that that
the PMOS is turned off when the current through it hits zero. The delay block is implemented
as a current-starved inverter which offers a relatively wide range of delay regulation and has a
simple structure as shown in Fig. 9.6.

**Buffering and level-shifting block**

The output signals from the PWM and current sensing blocks are used to control both switches.
The output signal of the PWM block is fed to drivers which consist of four stages of tapered
inverters in order to be able to drive the NMOS. The signal from the current sensing block is
either at 0 V or 1 V. However for the PMOS to be turned off reliably, the gate needs to be at a
potential higher than \( V_{OUT} - V_{T_p} \), preferably, at \( V_{OUT} \). The boosting of the signal is done using
capacitors \( C_1 \) and \( C_2 \), as shown in Fig. 9.7. The output signal of the current signal block is first
fed into a non-overlapping clock generator (NOCG), which outputs two non-overlapping clock signals, each feeding one of the two capacitors. Since $C_1$ is driving a much larger load, the gate of the power PMOS with a capacitance of around 6 pF, it has a value of about 60 pF. A MIM capacitor is the chosen design for this capacitor because its value is constant when the voltage across it changes. The area that $C_1$ occupies is $150 \, \mu m \times 200 \, \mu m$. The other capacitor, $C_2$, is about 1 pF. The last components of this block are the cross-coupled MOSFETs, $M_1$ and $M_2$. Both transistors are high-voltage devices, rated for 2.5 V operation, since the difference between the drain and source potentials can change by more than 1 V at startup and during transients when the load changes significantly. Transistor, $M_1$ is also made much larger than $M_2$. Since the sources of both transistors are at $V_{OUT}$, the voltage at $\phi_2$ tracks the output voltage, and this node swings between $V_{OUT}$ and $V_{IN}$.

Multiple advantages are achieved by using this technique. First, the drivers are implemented using standard devices, which saves power and improves speed. The second advantage is that all the drivers and the NOCG use the input voltage as the power supply and not the output voltage as in the traditional case where a level shifter is used, which improves the conversion efficiency.
Reference generation block

The reference generation block consists of a current reference block that provides a bias current for the operational amplifier, both comparators, and the ramp generator block. The current reference circuit schematic is shown in Fig. 9.8. The circuit consists of a current source block, where $M_1$, $M_2$, $M_3$, $M_4$ are sized to have relatively large channels in order to minimize the effect of the channel length modulation and therefore the supply dependence. This circuit has two stable states, for example, when the supply voltage $V_{DD}$ is turned on at start-up, if all of the transistors carry zero current, they may remain off indefinitely. This is resolved by means of the dynamic start up circuit, which drives the circuit out of the bias point where the bias current is zero.

9.1.5 Buck converter circuit design

The schematic of the buck converter with its control block is shown in Fig. 9.9. The filter capacitor used is a MIM capacitor with size $180 \mu m \times 200 \mu m$ and capacitance of $65 \text{ pF}$. Both switches are standard MOSFETs rated for $1 \text{ V}$ (nch, pch) from Table 9.1. The NMOS switch has a width of $96 \mu m$ and the feature length $60 \text{ nm}$, while the PMOS has a width of $120 \mu m$ and the same length. The switches are fed by $\phi_1$ and $\phi_2$ from the control block. The gates of $M_1$ and $M_2$ are switched between $V_{IN}$ and ground.
As with the boost converter, the control block takes in the same three input signals from off the chip, $V_{REF}$, $CLKREF$, and $CLKAUX$. The inductors for both converters are identical to those designed for the boost converters with the specifications reported in Table 9.2.

### 9.1.6 Buck control circuit design

The PWM control circuit diagram is reported in Fig. 9.10. This DCM PWM control system was designed and implemented occupying an area of about $100 \, \mu m \times 150 \, \mu m$. The operation is explained by means of its 5 sub-blocks as follows.

**PWM block**

This block generates a signal that controls the PMOS based on the output voltage level. The output voltage $v_{OUT}$ is applied to a type-II compensator along with a reference voltage $V_{REF}$ that is fed from off-chip and is used to set the output voltage level. The compensator consists of an operational amplifier with negative feedback through $Z_f$ and $Z_c$. For proper functioning of the compensator the values of resistors needed was fairly large to implement on chip ($100 – 500 \, k\Omega$). Therefore, switched capacitor configurations were used instead. The first switched capacitor circuit is shown in Fig. 9.11, in which a parasitic insensitive configuration is used. The two
Figure 9.10: The block diagram of the PWM control system of the buck converter.

Figure 9.11: The schematic of the feedback network of the error amplifier.
The compensation network of the error amplifier is implemented as shown in Fig. 9.12. The schematic uses the same technique to implement a resistor in series with capacitor $C_s$ and in parallel to $C_p$. The output of the operational amplifier $v_{Er}$ is then applied to a comparator along with a triangular waveform that is generated using a ramp generator. The output of the comparator yields a PWM signal that can be directly fed to the PMOS drivers. The PWM signal is also used in current sensing block as will be shown next.

**Clock generation block**

The clock generation block is identical to the one designed for the boost converter. It allows in a voltage to tune the frequency of the on-chip oscillator and at the same time works as the selector for a multiplexer that allows either the oscillator input to pass to the control circuit or an external clock that is fed by $CLKAUX$.

**Current sensing block**

Since the control is designed for DCM, the comparator should sense when the current falls down to zero and turn the NMOS off. The way this is implemented is by comparing the ground potential to the switching node voltage, hence changing state when the switching node hits zero, after this point the comparator is not needed until the next cycle. Therefore, the output of the PWM
block is used every cycle to reset the sense comparator (turning it on), after the on-time of the NMOS has elapsed the comparator is disabled until the following cycle.

**Buffering block**

Unlike the boost converter, both MOSFETs in a buck converter are switched between $V_{IN}$ and ground. Therefore, there is no need for level shifting in a buck converter. Both buffers are similar with each having four stages of tapered inverters, all of which use standard 1-V devices.

**Reference generation block**

The reference generation block is identical to the one designed for the boost converter (Fig. 9.8) generating around 5 $\mu$A.

### 9.2 Boost circuit simulations

In this section the simulation results using the circuit simulator Spectre from Cadence for the two boost converters are presented and compared in terms of conversion efficiency. The load and line regulation simulations are also reported.

#### 9.2.1 Converter with square inductor

The circuit consists of the square inductor shown in Fig. 9.3(a) integrated in the boost converter circuit of Fig. 9.4 and the PWM control loop of Fig. 9.5. The converter has an input voltage, $V_{IN}$, of 1 V in all simulations. The first simulation shows the relationship between the load current and the conversion efficiency for a constant output voltage. The output voltage, $V_{OUT}$, is kept at 2 V for a voltage gain of 2. A maximum conversion efficiency of 69% is achieved at a load current of 7 mA as shown in Fig. 9.13. It can also be seen that the efficiency decreases on either limit of the load current (output power) which is a typical property of the PWM control. At low output powers the switching losses become dominant since the switching frequency is constant. At high output powers conduction losses become dominant decreasing the efficiency.

The second simulation shows the relationship between the voltage gain and the conversion efficiency for a constant load current. The load current, $I_{OUT}$, is kept at 7 mA. A maximum conversion efficiency of 69.5% is achieved at a voltage gain of about 1.8 as shown in Fig. 9.14.
Figure 9.13: The load current $I_{OUT}$ versus the conversion efficiency of the square-inductor converter for a voltage gain of 2.

Figure 9.14: The voltage gain $V_{OUT}/V_{IN}$ versus the conversion efficiency of the square-inductor converter for a load current of 7 mA.
Figure 9.15: The voltage gain $V_{OUT}/V_{IN}$ versus the conversion efficiency of the square-inductor converter for different load currents.

Four different load currents were simulated in Fig. 9.15 to further show the relationship between the voltage gain and the conversion efficiency for multiple load currents. The dashed curve represents 5 mA load current, the solid curve is 7 mA, the dotted curve is 9 mA, and the dash-dotted curve is 11 mA.

### 9.2.2 Converter with chamfered inductor

The circuit consists of the chamfered inductor shown in Fig. 9.3(b) integrated with the boost converter circuit of Fig. 9.4 and the PWM control loop of Fig. 9.5. The converter has an input voltage, $V_{IN}$, of 1 V in all simulations. The first simulation shows the relationship between the load current and the conversion efficiency for a constant output voltage. The output voltage, $V_{OUT}$, is kept at 2 V for a voltage gain of 2. A maximum conversion efficiency of 73% is achieved at a load current of 7 mA as shown in Fig. 9.16.

The second simulation shows the relationship between the voltage gain and the conversion efficiency for a constant load current. The load current, $I_{OUT}$, is kept at 7 mA. A maximum conversion efficiency of 74% is achieved at a voltage gain of about 1.8 as shown in Fig. 9.17.
Figure 9.16: The load current $I_{OUT}$ versus the conversion efficiency of the chamfered-inductor converter for a voltage gain of 2.

Figure 9.17: The voltage gain $V_{OUT}/V_{IN}$ versus the conversion efficiency of the chamfered-inductor converter for a load current of 7 mA.
Figure 9.18: The voltage gain $V_{OUT}/V_{IN}$ versus the conversion efficiency of the chamfered-inductor converter for different load currents.

Four different load currents were simulated in Fig. 9.18 to further show the relationship between the voltage gain and the conversion efficiency for multiple load currents. The dashed curve represents 5 mA load current, the solid curve is 7 mA, the dotted curve is 9 mA, and the dash-dotted curve is 11 mA.

### 9.2.3 Comparisons

The first comparison in Fig. 9.19 shows the voltage gain versus the conversion efficiency for both converters. The converter with a square inductor is represented by the dashed curve, while the converter with a chamfered inductor is represented by the solid curve. Voltage gains ranging from 1.25 to 2.5 are simulated. The load current is kept constant at 7 mA and the input voltage at 1 V. As shown in Fig. 9.19, the converter with a chamfered inductor has a higher conversion efficiency throughout the whole range, with a maximum improvement of about 3.8%. The second comparison in Fig. 9.20 shows the load current versus the conversion efficiency for both converters. The converter with a square inductor is represented by the dashed curve, while the converter with a chamfered inductor is represented by the solid curve. Both the input and output voltages are kept constant at 1 V and 2 V, respectively. Load currents ranging from 1 mA to 25
Figure 9.19: A comparison of the voltage gain $V_{OUT}/V_{IN}$ versus the conversion efficiency for load current of 7 mA.

Figure 9.20: A comparison of the load current $I_{OUT}$ versus the conversion efficiency for a voltage gain of 2.
mA are simulated. The converter with a chamfered inductor has a higher conversion efficiency throughout the whole range, with a maximum improvement of about 5.6%.

### 9.2.4 Line and load regulation

Two simulations of the line regulation are shown in Fig. 9.21 and Fig. 9.22. The line regulation is a dynamic test that measures the ability of the output to remain constant given changes in the input voltage. $I_{OUT}$ is kept constant at 7 mA in both. The input voltage is varied between 0.9 V to 1.1 V in both simulations. In the first simulation in Fig. 9.21, the input voltage $V_{IN}$ is stepped from 0.9 V to 1 V and then to 1.1 V, each step is about 600 ns in length. In the second simulation, in Fig. 9.24, the input voltage is a sine wave with an amplitude of 100 mV, a minimum of 0.9 V and a maximum of 1.1 V, with a frequency of 1 MHz. The line regulation is about 1 %/V.

Two simulations of the load regulation are shown in Fig. 9.23 and Fig. 9.24. The load regulation is a dynamic test that measures the ability of the output to remain constant given changes in the load current. $V_{IN}$ is kept constant at 1 V in both. The output power is varied from 10 mW to 40 mW in both simulations. In the first simulation, Fig. 9.23, the load current $I_{OUT}$ is stepped from 5 mA to 12.5 mA and then to 20 mA, each transition occurs after about 600 ns. In the second simulation, Fig. 9.24, the load current is a sine waveform with an amplitude of 7.5 mA, a minimum of 5 mA and a maximum of 20 mA, with a frequency of 1 MHz. The load regulation is about 10 %/A.
Figure 9.22: The output voltage for a line voltage changing from 0.9 V to 1.1 V with a frequency of 1 MHz.

Figure 9.23: The output voltage for load current steps from 5 mA to 20 mA.
Transient Response

<table>
<thead>
<tr>
<th>time (us)</th>
<th>I (mA)</th>
<th>V (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>22.5</td>
<td>3.0</td>
<td>2.5</td>
</tr>
<tr>
<td>20.0</td>
<td>2.5</td>
<td>2.0</td>
</tr>
<tr>
<td>17.5</td>
<td>2.0</td>
<td>1.5</td>
</tr>
<tr>
<td>15.0</td>
<td>1.5</td>
<td>1.0</td>
</tr>
<tr>
<td>12.5</td>
<td>1.0</td>
<td>.5</td>
</tr>
<tr>
<td>10.0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>7.5</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>5.0</td>
<td>0</td>
<td>2.5</td>
</tr>
<tr>
<td>2.5</td>
<td>0</td>
<td>2.0</td>
</tr>
</tbody>
</table>

Figure 9.24: The output voltage for a load current changing from 5 mA to 20 mA with a frequency of 1 MHz.

### 9.3 Buck circuit simulations

In this section the simulation results using the circuit simulator Spectre from Cadence for the two buck converters are presented and compared in terms of conversion efficiency. The load and line regulation simulations are also reported.

#### 9.3.1 Converter with square inductor

The circuit consists of the square inductor shown in Fig. 9.3(a) integrated with the buck converter circuit of Fig. 9.9 and the PWM control loop of Fig. 9.10. The converter has an input voltage, $V_{IN}$, of 1 V in all simulations. The first simulation shows the relationship between the load current and the conversion efficiency for a constant output voltage. The output voltage, $V_{OUT}$, is kept at 500 mV for a voltage gain of 0.5. A maximum conversion efficiency of 70% is achieved at a load current of 27 mA as shown in Fig. 9.25. It can also be seen that the efficiency decreases on either limit of the load current (output power) which is a typical property of the PWM control. At low output powers the switching losses become dominant since the switching frequency is constant. At high output powers conduction losses become dominant decreasing the efficiency.

The same simulation is repeated for a different voltage gain in Fig. 9.26. The output voltage,
Figure 9.25: The load current $I_{OUT}$ versus the conversion efficiency of the square-inductor buck converter for a voltage gain of 0.5.

Figure 9.26: The load current $I_{OUT}$ versus the conversion efficiency of the square-inductor buck converter for a voltage gain of 0.75.
Figure 9.27: The voltage gain $V_{OUT}/V_{IN}$ versus the conversion efficiency of the square-inductor buck converter for a load current of 30 mA.

$V_{OUT}$ is kept at 750 mV for a voltage gain of 0.75. A maximum conversion efficiency of 76% is achieved at a load current of 50 mA.

The third simulation shows the relationship between the voltage gain and the conversion efficiency for a constant load current. The load current, $I_{OUT}$, is kept at 30 mA. A maximum conversion efficiency of 75% is achieved at a voltage gain of about 0.7 as shown in Fig. 9.27.

### 9.3.2 Converter with chamfered inductor

The same simulations were run for the second buck converter with the chamfered inductor (shown in Fig. 9.3(b)). The first simulation shows the relationship between the load current and the conversion efficiency for a constant output voltage. The output voltage, $V_{OUT}$, is again kept at 500 mV for a voltage gain of 0.5. A maximum conversion efficiency of 73% is achieved at a load current of 30 mA as shown in Fig. 9.28.

The same simulation is repeated for a different voltage gain in Fig. 9.29. The output voltage, $V_{OUT}$, is kept at 750 mV for a voltage gain of 0.75. A maximum conversion efficiency of 79% is achieved at a load current of 50 mA.
Figure 9.28: The load current $I_{OUT}$ versus the conversion efficiency of the chamfered-inductor buck converter for a voltage gain of 0.5.

Figure 9.29: The load current $I_{OUT}$ versus the conversion efficiency of the chamfered-inductor buck converter for a voltage gain of 0.75.
Figure 9.30: The voltage gain $V_{OUT}/V_{IN}$ versus the conversion efficiency of the chamfered-inductor buck converter for a load current of 30 mA.

The third simulation shows the relationship between the voltage gain and the conversion efficiency for a constant load current. The load current, $I_{OUT}$, is kept at 30 mA. A maximum conversion efficiency of 78% is achieved at a voltage gain of about 0.7 as shown in Fig. [9.30].

### 9.3.3 Comparisons

The first comparison in Fig. [9.31] shows the voltage gain versus the conversion efficiency for both converters. The converter with a square inductor is represented by the dashed curve, while the converter with a chamfered inductor is represented by the solid curve. Voltage gains ranging from 0.4 to 0.8 are simulated. The load current is kept constant at 30 mA and the input voltage at 1 V. As demonstrated, the converter with a chamfered inductor has a higher conversion efficiency throughout the whole range, with a maximum improvement of about 4.2%.

The second comparison in Fig. [9.32] shows the load current versus the conversion efficiency for both converters. The converter with a square inductor is represented by the dashed curve, while the converter with a chamfered inductor is represented by the solid curve. Both the input and output voltages are kept constant at 1 V and 0.5 V, respectively. Load currents ranging from 8 mA to 60 mA are simulated. As evident from Fig. [9.32] the converter with a chamfered inductor
Figure 9.31: A comparison of the voltage gain $V_{OUT}/V_{IN}$ versus the conversion efficiency for load current of 30 mA.

Figure 9.32: A comparison of the load current $I_{OUT}$ versus the conversion efficiency for a voltage gain of 0.5.
has a higher conversion efficiency throughout the whole range, with a maximum improvement of about 4.8%.

The third comparison in Fig. 9.33 also shows the load current versus the conversion efficiency for both converters. Both the input and output voltages are kept constant at 1 V and 0.75 V, respectively. Load currents ranging from 8 mA to 60 mA are simulated. As can be seen, the converter with a chamfered inductor has a higher conversion efficiency throughout the whole range, with a maximum improvement of about 3.8%.

9.4 Discussion

By observing the simulation results comparing the square inductor to the chamfered inductor for both the boost and buck converters. The conversion efficiency improvement was between 3.8% and 5.6%. This improvement was expected by the analytical results provided in Chapter 7. The chamfered inductor provides a higher inductance time-constant ratio $L/R$ which is directly proportional to the power loss of a converter. Therefore, having a higher inductance time-constant ratio increases the overall conversion efficiency as evident from the results provided. This applies for both converters and for different ranges of output powers.
Table 9.3: Boost converter performance summary and comparisons.

<table>
<thead>
<tr>
<th>Design</th>
<th>[8]</th>
<th>[9]</th>
<th>[5]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.18-μm CMOS</td>
<td>0.18-μm CMOS</td>
<td>0.13-μm CMOS</td>
<td>65-nm CMOS</td>
</tr>
<tr>
<td>Area (mm²)</td>
<td>0.127</td>
<td>1.69</td>
<td>2.25</td>
<td>0.5</td>
</tr>
<tr>
<td>L (nH)</td>
<td>34.4</td>
<td>20</td>
<td>11</td>
<td>8.5</td>
</tr>
<tr>
<td>V_{IN} (V)</td>
<td>1.8</td>
<td>1.6 – 2.6</td>
<td>1.2</td>
<td>0.9 – 1.1</td>
</tr>
<tr>
<td>V_{OUT} (V)</td>
<td>8 – 10</td>
<td>2 – 15</td>
<td>2.4 – 3.3</td>
<td>1.2 – 2.4</td>
</tr>
<tr>
<td>P_{OUT} (mW)</td>
<td>6.4</td>
<td>3.6</td>
<td>34</td>
<td>50</td>
</tr>
<tr>
<td>f_{SW} (MHz)</td>
<td>1400</td>
<td>120</td>
<td>80 – 220</td>
<td>100</td>
</tr>
<tr>
<td>η</td>
<td>19</td>
<td>28</td>
<td>45</td>
<td>75</td>
</tr>
</tbody>
</table>

Table 9.4: Buck converter performance summary and comparisons.

<table>
<thead>
<tr>
<th>Design</th>
<th>[30]</th>
<th>[12]</th>
<th>[31]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.13-μm CMOS</td>
<td>0.18-μm CMOS</td>
<td>0.13-μm CMOS</td>
<td>65-nm CMOS</td>
</tr>
<tr>
<td>Area (mm²)</td>
<td>3.375</td>
<td>2.5</td>
<td>4</td>
<td>0.5</td>
</tr>
<tr>
<td>L (nH)</td>
<td>9.8</td>
<td>4.38</td>
<td>10.5</td>
<td>8.5</td>
</tr>
<tr>
<td>V_{IN} (V)</td>
<td>2 – 2.6</td>
<td>2.2</td>
<td>3.3</td>
<td>0.9 – 1.1</td>
</tr>
<tr>
<td>V_{OUT} (V)</td>
<td>1.1 – 1.5</td>
<td>0.75 – 1</td>
<td>1.2 – 2.5</td>
<td>0.4 – 0.8</td>
</tr>
<tr>
<td>P_{OUT} (mW)</td>
<td>180</td>
<td>55</td>
<td>288</td>
<td>45</td>
</tr>
<tr>
<td>f_{SW} (MHz)</td>
<td>200</td>
<td>660</td>
<td>180</td>
<td>100</td>
</tr>
<tr>
<td>η</td>
<td>52</td>
<td>31</td>
<td>70</td>
<td>82</td>
</tr>
</tbody>
</table>
We also compared both the chamfered-inductor based boost and buck converters designed here to the integrated implementations reported in the literature. Table 9.3 shows the boost converter comparison, as can shown the conversion efficiency of the boost converter we designed is about 30% higher than those reported. Our design can provide higher output power at a footprint that is smaller than almost all of the designs. The switching frequency and voltage conversion ratio are also comparable to most of the designs. There are multiple reasons for this performance improvement. On an inductor-design level, the geometry optimization provided in improvement in comparison to both the square and the octagon shapes that are used in the previously implemented converters. Additionally, the optimization algorithm that we developed also maximized the inductance time-constant ratio which in turn improved the conversion efficiency. On a circuit-design level, the proposed booster circuit for controlling the gate of the PMOS without using any output power and eliminating crowbar current also helped increase the efficiency. In addition, optimizing the tapered buffer that control both switches along with optimizing the layout of the switches to reduce the parasitics also aided in increasing the conversion efficiency.

The designed buck converter also showed higher conversion efficiencies in comparison to the literature as shown in Table 9.4. Our design occupies a smaller area than all the previously reported designs, with a comparable voltage conversion ratio and output power. The conversion efficiency of our design is higher by about 12%. Again, this performance improvement was achieved due to a combination of inductor optimization and design techniques.

This performance improvement will help in realizing more powerful and advanced wearable, portable, sensor, and IoT devices. By focusing on fully-integrated implementations (traditionally limited to specific applications), parametric power converter design blocks that can be easily scaled (to meet technological constraints and power levels requirements), simulated, and dropped into any digital chip design to greatly widen its acceptable power supply range and voltage tolerance can be created. Such designs will significantly reduce the cost and complexity of building heterogeneous multi-chip systems. Eventually, better performance and efficiency of mobile IoT applications (constrained by power or voltage levels) will be achieved through the design flexibility of on-chip converters and power processing. The new knowledge gained by our converter designs is extremely valuable, as it not only introduces a design methodology for fully-integrated implementations, but also demonstrates the feasibility of integrating all the components of power converters on a single chip.
9.5 Summary

In this chapter, the chip design was discussed in detail. The fabrication technology, tools, and design flow used are presented in the first section. The specifications of the designed inductors, switches, and control blocks for both converters are all provided. The simulation results of the two designed boost converters are shown and compared in the second section, while in the third section, the simulation results of the two buck converters are shown and compared as well.
Chapter 10

Conclusions

One of the main contributions of this work was to prove the feasibility of realizing fully-integrated dc-dc converters. Complete models designed specifically for integrated dc-dc converters were derived and formulated. In addition to the description of the model, the effects of the parasitics, specifically those relevant to integrated converters, are discussed extensively.

Integrated inductors have been used for years in radio frequency applications, therefore the existing models target those applications and are not suitable for power converters. The second main contribution was the modelling of integrated inductors for power converters. This was done by using different methods to calculate the inductance and the parasitic resistance (the main power loss of integrated inductors for power converters). We introduced the inductance time-constant ratio, a term that assesses the performance of an inductor. By changing the geometry of the inductor we were able to maximize the performance of the inductor and hence the overall conversion efficiency of the converter.

The third main contribution of this work was to combine the model of the converter with the one of the inductor and develop an optimization algorithm that maximizes the conversion efficiency. Optimizing the overall conversion efficiency was the main goal of this work.

This work helped enable using integrated inductors for building dc-dc converters, that are fully integrated, low-power, and efficient. The work also helped establishing the basis for more complex models of integrated inductors that are dedicated for power converters. The models developed were used to deduct important trade-offs which could potentially help designers easily choose design parameters without the need to run a large number of circuit simulations. The optimization algorithm developed will also help shorten the design time by having an estimate of the overall efficiency and the different power losses associated with the different components.
10.1 Future work

The models provided in this work can be scaled up or down based on the application. Some potential applications that can use integrated converters are portable and wearable devices and sensors. Since the consumed power and size have to be kept at a minimum and the output power levels required are usually low, the converter and inductor sizes could be scaled down without sacrificing efficiency. Alternatively, for applications that require higher load such as touch screen readout channels the converters can be scaled up to achieve the required output power at a high efficiency.

The inductor’s model that was developed for this work has been tested for both TSMC 180-µm and TSMC 65-nm technologies, and proved functional for both. It was tested for a range of frequencies from 80 to 300 MHz. While this was sufficient for the purposes of this research, it could also be tested for more fabrication technologies and at a wider frequency range. The performance of an integrated inductor is highly dependent on the fabrication technology. All the inductors designed for this work used the available standard TSMC 65-nm technology which provides, one thick metal layer made of copper for implementing inductors. Based on the models developed, we expect that newer technologies would also benefit from the model to estimate and achieve higher performance.

Aside from the models, the power switches also become a critical challenge especially for boost converters for two main reasons: driving voltage and device constraints. For driving voltages and especially for the PMOS in a boost converter, different techniques could be developed in order to reliably switch it on and off. In this work a boosting capacitor was connected in series with the gate and the gate of the PMOS was switched between the input and output levels to minimize the switching losses. Other techniques for boosting can be investigated using different level-shifter circuits that might further reduce losses. The device constraints are related to the fabrication technology, the TSMC 65-nm offers high voltage devices that can withstand up to 2.5 V, however, the threshold voltage of these devices is relatively high and the feature length is significantly larger than the standard devices. This results in the power transistors occupying a relatively large area and consuming a significant amount of power to be driven. Different technologies might offer better high voltage devices. Device stacking (i.e. connecting multiple standard MOSFETs in series) is also another option that is worth investigating.

The choice of control circuitry is essential in ensuring proper functioning of the converters. In this work a fast PWM control was implemented that is effective for the range of load currents required. Other control schemes can be investigated and compared with respect to overall performance. More complex designs, such as a combination of both a PWM and PFM controls should be studied further. This offers an adaptable control where the PFM takes over at lower loads and PWM at higher loads, optimizing the overall efficiency.
References


Appendix A

Published papers

A.1 Refereed conference publications


### A.2 Refereed journal publications