High-Efficiency Integrated Switched-Capacitor Power Converters with Capacitor-Bank Charge Reuse

by

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A Thesis
presented to
The University of Guelph

In partial fulfilment of requirements
for the degree of
Master of Applied Science
in
Engineering

Guelph, Ontario, Canada

ABSTRACT

HIGH-EFFICIENCY INTEGRATED SWITCHED-CAPACITOR POWER CONVERTERS WITH CAPACITOR-BANK CHARGE REUSE

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This thesis investigates the design trade-offs and methods of implementing charge reuse in switched-capacitor power converters resulting in improved power conversion efficiency. A detailed analysis of the process of charge reuse and its relation with power savings is included. The use of an auxiliary capacitor bank structure for improving efficiency is investigated, and the resulting design trade-offs are explored. A dual-access capacitor bank circuit is presented, which results in a factor of four reduction in the capacitor bank area, at no cost to the designer. The capacitor bank structure is simulated and verified using a voltage doubler designed in 65 nm integration technology. The results of the simulations show a peak power conversion efficiency of 90%, which indicates a 5% improvement when compared to a conventional voltage doubler without charge reuse. Lastly, in order to address the timing constraints associated with charge reuse, a dynamic biasing method is proposed. The dynamic biasing technique results in a decreased on resistance of the switches, and the simulations indicate that the equalization time can be reduced by as much as a factor of 20. All of the proposed techniques combine to make reducing the dynamic losses on parasitic capacitors simple and well modelled, while resulting in improved performance.

Acknowledgments

I'd like to offer a big thanks to Professor Stefano Gregori for his patience, time, and assistance as well as giving me the opportunity to pursue my research. I'd also like to thank Professor Petros Spachos for his guidance, and continued positivity.

Lastly, I'd like to thank my friends and family for their encouragement and support.

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List of Abbreviations

- BPE - Bottom Plate Equalization
- CMOS - Complementary Metal Oxide Semiconductor
- EMI - Electromagnetic Interference
- IO - Input Output
- MIM - Metal Insulator Metal
- MOM - Metal Oxide Metal
- MOS - Metal Oxide Semiconductor
- PCB - Printed Circuit Board
- SC - Switched Capacitor
- SCPC - Switched-Capacitor Power Converter
- TPE - Top Plate Equalization
- TSMC - Taiwan Semiconductor Manufacturing Company

List of Symbols

- V_{IN} - Converter Input Voltage
- V_{OUT} - Converter Output Voltage
- C_{Fly} - Flying capacitance
- α_T - Ratio between parasitic top plate capacitance and flying capacitance
- α_B - Ratio between the parasitic bottom plate capacitance and flying capacitance
- f_{SW} - Switching frequency of the converter
- T_{SW} - Switching period of the converter, the inverse of f_{SW}
- N - Number of converter stages
- S - Number of soft charging phases
- T_i - Number of time-interleaved cores

Chapter 1

Introduction

1.1 Overview of Integrated Power Converters

Power converters refer to circuits which take one incoming voltage and transform it into another. Specifically, they use energy storage elements such as the capacitor and inductor in order to transform the incoming voltage. Integrated power converters involve the use of integrated components, typically to control the way in which the energy storage elements are interfaced, and to provide some regulation of the output. Power converters have a defined range of load powers which they can deliver, after which the output voltage will begin to vary from the desired value. Additionally, power converters have an efficiency which relates the amount of power output, to the amount of input power to the circuit, giving a measure of how much energy is wasted.

Switched-capacitor power converters (SCPC) involve storing a voltage on a capacitor, then changing the voltages on the top and bottom plates of the capacitor to generate a new voltage. The control of the top and bottom plate voltages is performed using transistors along with control circuitry, where the transistors are switched frequently to deliver power.

1.2 Motivation

Power efficiency is an increasingly important performance parameter in modern electronic circuits, given the rise of green computing technology and mobile devices. Mobile devices have a requirement that their power consumption be minimized, as this can reduce the size of the battery, reducing the cost and size of a device [1].

Modern electronic circuit can improve efficiency and performance by providing different parts of the system with unique supply voltages. For example, analog electronics and sensors typically require a substantially different voltage than digital logic. This presents an issue for many circuit designers, as many systems have one supply voltage in the form of a single source, which does not give them the ability to modulate the supply voltage for the unique components. Additionally, the voltage output of most sources is variable over time, which can be problematic for functions which are sensitive to changes in supply voltage.

In order to address the issues associated with having a single source for a system, power converters take the main voltage supply and generate a different voltage based on it using either inductors, capacitors or a combination of the two. This can meet the supply voltage needs of the numerous functions of a system, as well as compensate for the variability in supply from the sources themselves. Many implementations of power converters involve discrete energy storage elements in order to maximize power output. However, not all applications require the large output powers associated with discrete components, and would instead benefit from solutions with fewer, less area expensive components designed around lower output powers [2].

Another trend present in modern electronic circuits relates to the supply voltage of microprocessors, which has been progressively decreasing. Despite the supply voltage of microprocessors decreasing, their power consumption has not been substantially reduced. A consequence of this is that modern microprocessors have a substantial number of their input output (IO) pins

dedicated to delivering the power for the chip, in order to meet the supply current demands in an efficient manner. One method of addressing this issue would be to supply the microprocessor with a higher supply voltage, then step it down on chip. This would reduce the amount of current which is passed through the IO pins, and allow for a better transmission of power into the chip.

Both microprocessor and single supply systems can have many of their power supply challenges improved by using fully-integrated power conversion. Microprocessor systems which step down the voltage on chip fundamentally require fully-integrated circuits, as any discrete energy storage elements would require their own pins, eliminating the benefits from such a solution. There are a number of improvements for single-supply systems requiring multiple voltage levels. The first is that the design complexity at the level of the printed circuit board (PCB), is reduced, as there are fewer components to route, which results in a reduction in area, saving cost. Additionally, there is also the fact that discrete components simply require area themselves, so fully-integrated circuits can further reduce cost in this way. Lastly, there are issues associated with electromagnetic interference (EMI), where discrete components create a high level of interference [3].

Fully-integrated power converters have their own set of design challenges, as many of the on-chip storage elements have their own associated issues. Fully-integrated capacitors present excellent power scaling, as well as being available in most fabrication processes, though they have challenges associated with their density and parasitic capacitances. Planar on chip inductors are lossy without the addition of special fabrication steps, and will be highly dependent on the number of metal layers as well as several other factors [4, 5]. As a result, switched-capacitor power converters appear to be the most promising method of meeting the needs of fully-integrated power converters.

One of the ways to address the challenges associated with SCPCs are circuit level techniques. The highly interconnected nature and additional control

over the topology of integrated SCPC give designers the ability to make maximal use of the capacitors and transistors in a given technology, substantially improving performance.

1.3 Objective

The objective of the thesis is to investigate methods of improving the performance of fully-integrated SCPC through the use of circuit level techniques. Specific focus is given to the reduction of the impact of parasitic capacitances, while investigating the associated trade-offs with such a technique. Improvements and alternate methods of implementing these techniques are discussed, as well as methods of minimizing the associated area overhead of such circuits.

1.4 Methods

The methods used to investigate improvements into improving SCPC are as follows. First a literature review is performed in order to establish background on the topic. Then different methods of improvement are investigated, starting from the fundamental circuit theory, doing analysis and calculations, verifying with idealized circuit simulations, and eventually simulating the proposed solutions using CMOS 65 nm technology.

1.5 Contributions

The contributions presented in this thesis are an analysis of charge reuse for a generic number of stages, investigating their impact on SCPC operation. Additionally, the timing and control of charge reuse structures is investigated. Next, a method of implementing charge reuse is presented which makes use of a capacitor bank circuit. The structure is then analyzed, the associated area trade-offs are investigated, and improvements are proposed. Lastly, a method of dynamically biasing the equalization transistors used for charge reuse is investigated, along with the associated benefits.

1.6 Thesis Organization

The rest of the thesis is organized as follows. Chapter 2 contains background research and the literature review of existing techniques and improvements. Chapter 3 features a comprehensive analysis of charge reuse, covering the benefits, as well as the associated design trade-offs. Chapter 4 features an analysis of the capacitor bank implementation of charge reuse, where the charge reuse is implemented using an auxiliary bank of capacitors. Chapter 5 focuses on a novel method of biasing transistors in SCPCs to minimize the design trade-offs associated with charge reuse.

Chapter 2

Background Information and Literature Review

2.1 SC Power Converter Background

Switched-capacitor power converters operate by taking an incoming voltage, storing it on a capacitor, then modifying the configuration, so that the capacitor is placed in series with another voltage. This allows for the generation of a higher or lower voltage in an efficient manner. SCPCs can both increase or decrease an incoming voltage, decreasing the incoming voltage is referred to as "buck" operation, while increasing it is referred to as "boost" operation.

2.2 Design Requirements and Challenges

SCPCs serve to provide a method of taking an input voltage provided to the converter and multiplying it by a discrete value - typically referred to as the gain of the converter. The generated voltage have zero output resistance, and be stable regardless of the input voltage. The cost of such a system can be assessed based on the silicon area occupied by the converter. The main design parameters are as follows:

2.2.1 Power Density

The power density of a converter is a measure of how much power it can output per unit area. The power density of an SCPC is determined by the capacitance density of the flying capacitors, the circuit topology used, and the operating frequency of the converter [6].

2.2.2 Output Voltage Ripple

Output voltage ripple refers to the variation in the output voltage with respect to time, typically associated with the discrete state changes of the converters. High levels of output ripple are undesirable, as power supply noise can degrade the quality of analog electronics, or produce computational errors in digital logic.

2.2.3 Conversion Efficiency

The power efficiency of converters is determined by the ratio between the output power and the input power of the circuit [7].

2.2.4 Startup Time

The startup time is a measure of how long the converter takes to drive the output from 0 to V_{OUT}. This is an especially prominent metric when dealing with systems that frequently change their desired output voltage, such as in flash memory chips.

2.2.5 Conversion Ratio

The conversion ratio of the converter is a measure of the ratio between its input and output voltages.

2.3 Types of Switched-Capacitor Power Converters

There are a number of SCPC circuit configurations that can be employed to convert one voltage to another. However, some are more suitable for fully-integrated circuits as a result of certain design constraints. The circuit configuration used throughout the thesis it the voltage doubler, largely as it has constant transistor stresses independent of the number of stages [8],[9]. A schematic of the voltage doubler can be seen in Figure 2.1, which can be placed in series to further increase the conversion ratio. A schematic of a 2-stage doubler is in Figure 2.2. The relationship between voltage stress on the capacitor and the output for the boost configuration is,

$$V_C = V_{OUT} - V_{IN}, \tag{2.1}$$

while the maximum voltage stress in the buck configuration is,

$$V_C = V_{IN} - V_{OUT}. \tag{2.2}$$

The ideal, lossless conversion ratio relating the input to the output is determined by the number of doubler stages (N), where

$$V_{OUT} = (N+1)V_{IN}, \tag{2.3}$$

in the boost configuration, and

$$V_{IN} = (N+1)V_{OUT}, \tag{2.4}$$

in the buck configuration. This conversion ratio will vary in a real context, depending on the load currents, and the parasitic capacitances in the converter.

2.4 Basic SC Converter Operation

The basic operation of an SC power conversion cell can be described with reference to Figure 2.3a. Figure 2.3b contain all of the components which can

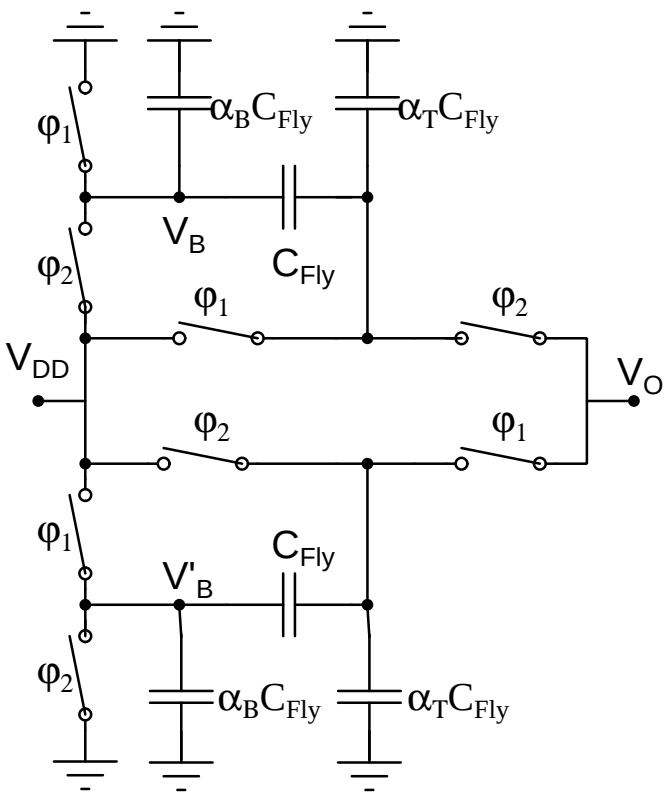


Figure 2.1: Schematic of the single stage voltage doubler using ideal switches

be used to fully understand many of the challenges to the designer, as well as some of the bottlenecks in the system. The function of the cell involves switching the top plate of the capacitor between V_{T2} and V_{T1} and the bottom plate between V_{B2} and V_{B1}. The flying capacitor stores the voltage difference between these states, and effectively adds that to one of the voltages, generating a new voltage level. Lastly, the stray capacitances to ground α_T and α_B are a result of non-idealities in the flying capacitor, where there is capacitance to the substrate ground, as well as other nodes in the circuit. Typically, α_T and α_B degrade performance by reducing the efficiency and output voltage of the circuit, so it is desirable to have them as small as possible.

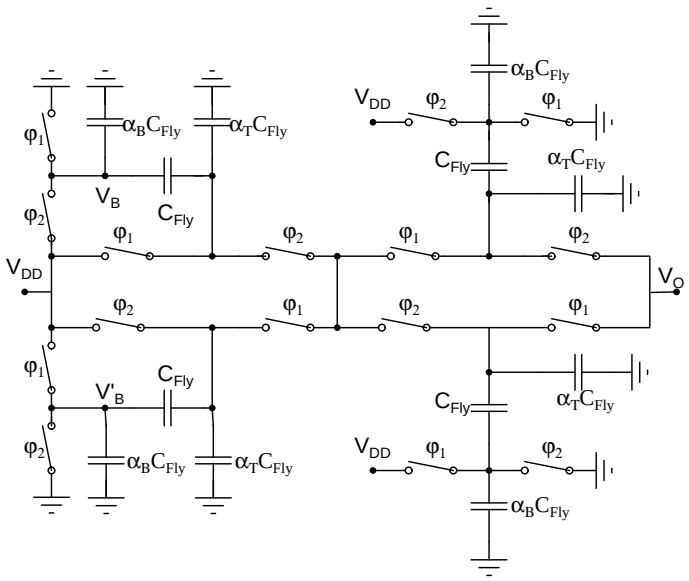
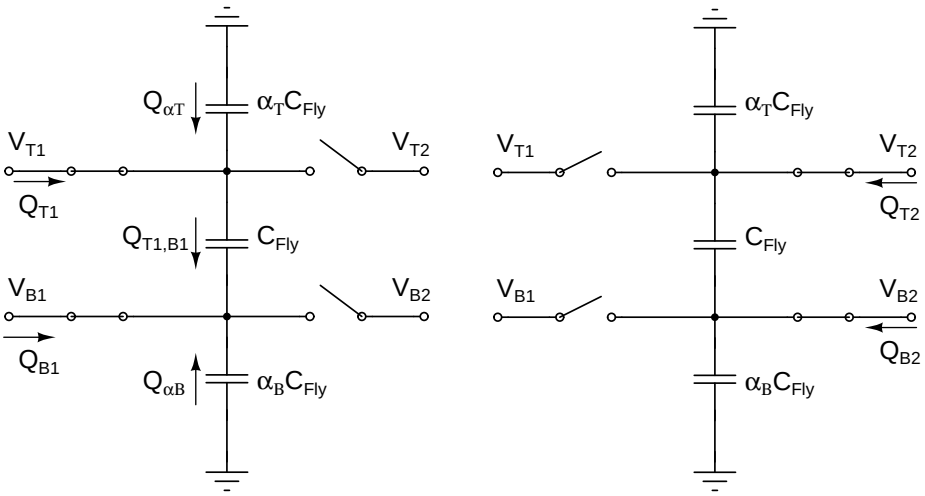


Figure 2.2: Schematic of a two stage voltage doubler, implemented using ideal switches



(a) Phase 1, capacitor stores $V_{T1} - V_{B1}$. (b) Phase 2, capacitor stores $V_{T2} - V_{B2}$.

Figure 2.3: Fundamental switched-capacitor cell.

2.4.1 Phase 1

The analysis begins with a few assumptions, first it is assumed that the analysis is performed at steady state, additionally it is assumed that the capacitances involved are all linear, and that there is enough time for a full charge and discharge cycle to occur. The operation is as follows, the capacitor is charged in the first phase, storing a voltage of $V_{T1} - V_{B1}$. This involves current flowing through the flying capacitor and the switches, resulting in an RC time constant which determines the amount of time required for complete charge transfer. Additionally, current is required to charge the top plate parasitic capacitance from V_{T2} to V_{T1}, as well as the charging of α_B.

The amount of charge flowing through the flying capacitor from V_{T1} to V_{B1} is,

$$Q_{T1,B1} = C_{Fly}(V_{T,1} - V_{T,2} + V_{B2} - V_{B,1}), \tag{2.5}$$

while the charge through the top plate parasitic capacitor from $V_{T,1}$ is,

$$Q_{\alpha T} = \alpha_T C_{Fly}(V_{T,2} - V_{T,1}), \tag{2.6}$$

and the charge through the bottom plate parasitic capacitance to V_{B1} is,

$$Q_{\alpha B} = \alpha_T C_{Fly}(V_{B,2} - V_{B,1}). \tag{2.7}$$

The resulting charge from $V_{T,1}$ is the sum of $Q_{T1,B1}$ and $Q_{\alpha T}$,

$$Q_{T1} = C_{Fly}\left(V_{T,1} - V_{T2} + V_{B2} - V_{B,1} - \alpha_T(V_{T,2} - V_{T,1})\right), \tag{2.8}$$

while the resulting charge flow from $V_{B,1}$ is determined based on $Q_{T1,B1}$ and $Q_{\alpha B}$,

$$Q_{B1} = C_{Fly}\left(V_{T,2} - V_{B,2} - V_{T,1} + V_{B,1} - \alpha_T(V_{B,2} - V_{B,1})\right). \tag{2.9}$$

2.4.2 Phase 2

The switched-capacitor cell configuration in the second phase can be seen in Figure 2.3b. The second phase can be understood somewhat easily with

respect to phase 1, as current flows from V_{T1} to V_{T2} at steady state, as the flying and parasitic capacitors block DC current. Likewise the current that flows into V_{B1} must flow out of V_{B2}. From this $Q_{T2} = -Q_{T1}$, and $Q_{B2} = -Q_{B1}$, which allows a designer to express the energy drawn from each node, for example

$$E_{T1} = V_{T1}Q_{T1}. \tag{2.10}$$

2.4.3 Boost Example

An example can be made for the boost converter case, in which $V_{T1} = V_{DD}$, $V_{T2} = V_{OUT}$, $V_{B1} = 0$ and $V_{B2} = V_{DD}$, where V_{DD} is the supply voltage. The output power can be calculated by taking the energy delivered to the output, and multiplying it by the switching frequency,

$$P_{OUT} = -E_{T2}f_{SW} = f_{SW}C_{Fly}V_{OUT}\left(2V_{DD} - V_{OUT} - \alpha_T(V_{OUT} - V_{DD})\right). \tag{2.11}$$

One of the definitions which can be useful is to describe the output voltage of a converter configuration with reference to its idealized conversion ratio. The output voltage can be described for a single stage as,

$$V_{OUT} = 2V_{DD} - \Delta V, \tag{2.12}$$

and ΔV is the voltage drop from the ideal ratio. The output power described in reference to ΔV is,

$$P_{OUT} = f_{SW}C_{Fly}(2V_{DD} - \Delta V)\left(\Delta V - \alpha_T(V_{DD} - \Delta V)\right), \tag{2.13}$$

which will describe the output current in terms of the voltage drop, giving an almost linear relationship between output power and ΔV.

2.4.4 Sources of Power Loss

The first source of loss which is especially prominent in fully-integrated SCPC are the **capacitive losses** in the converter. The capacitive losses will specifically refer to the losses which are a result of charging the parasitic capacitances

in a SCPC. These parasitic capacitances are typically dominated by the α_T and α_B of the flying capacitor, though they can include losses associated with the transistors.

A basic approximation of both the top and bottom plate losses can be acquired by assuming that the change in voltage between each state on each of them is V_{DD}. From this the power loss on the parasitic plate capacitors is,

$$P_{par} = f_{SW} C_{Fly} (\alpha_B V_{DD}^2 + \alpha_T (V_{OUT} - V_{DD})^2) \tag{2.14}$$

The next source of loss which is present in SCPC are the losses associated with the movement of charge through the switches. These losses will be referred to as **resistive losses** throughout the text, which will refer specifically to the losses induced by current flow through the flying capacitor. In order to conceptually understand the resistive losses in SCPC, first the relationship between current and time must be understood. The current during the charging and discharging phases can be approximated as a decaying exponential, where

$$I = \frac{\Delta V}{R} \exp\left(\frac{-t}{RC_{Fly}}\right), \tag{2.15}$$

where R is the total resistance in the charge path. Next recall from classical circuit theory that the power dissipated on a resistor is,

$$P = I^2 R. \tag{2.16}$$

The resistive losses during the discharge can be acquired by taking the integral of the power over a full charge or discharge period,

$$\begin{aligned} P_{res} &= \frac{2}{T_{SW}} \int_0^{T_{SW}/2} \left(\frac{\Delta V}{R} \exp\left(\frac{-t}{RC_{Fly}}\right)\right)^2 R dt \\ &= f_{SW} \Delta V^2 C_{Fly} \left(1 - \exp\left(\frac{-T_{SW}}{RC_{Fly}}\right)\right), \end{aligned} \tag{2.17}$$

however, as a full charge or discharge is assumed, then

$$P_{res} = f_{SW} \Delta V^2 C_{Fly}, \tag{2.18}$$

which indicates that the resistive losses are independent of the switch resistance. An alternate method of quickly approximating resistive losses is to use the metric of either **mean squared current** (I_{MS}) or **root mean squared current** (I_{RMS}). The mean squared current is a measure of the average squared current over a time interval and can be calculated,

$$I_{MS} = \frac{1}{T}\int_0^T I^2 dt. \tag{2.19}$$

The root mean squared current is simply the square root of I_{MS}, where

$$I_{RMS} = \sqrt{I_{MS}} = \sqrt{\frac{1}{T}\int_0^T I^2 dt}. \tag{2.20}$$

Both I_{MS} and I_{RMS} can be used to approximate the resistive losses, as I_{MS} is directly related to the average resistive losses on a resistor, assuming R is time invariant.

2.4.5 Efficiency and Output Power

Next the relationship between the capacitive losses, resistive losses, and output power can be investigated [10]. The expression for output power is (2.13), indicating that for small ΔV, the output power is proportional to the output current. A graph of output power, capacitive losses, and resistive losses is provided for varying values of ΔV in Figure 2.4. The quadratic nature of the resistive losses is evident, as well as the roughly linear nature of the output power with respect to ΔV. The peak efficiency occurs around the point where the capacitive losses equal the resistive losses, higher values of ΔV than this are dominated by resistive losses, while lower values are predominantly capacitive losses. The scaling of the resistive and capacitive losses relative to the output power is available in Figure 2.5.

This creates something of a dilemma for the designer, as the maximum efficiency of the system is limited entirely by the value of α_B and α_T. Additionally, there is little that can be done in this circuit configuration to improve the relationship between output power and resistive losses. The frequency can

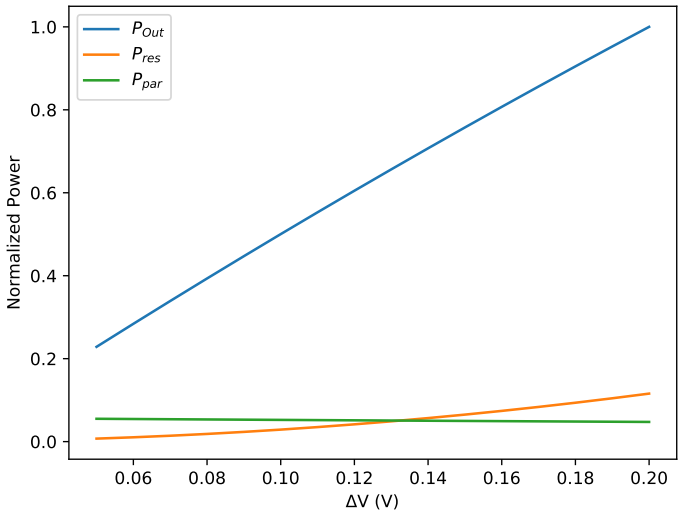


Figure 2.4: Normalized power graph for a SC converter cell with $\alpha_T = 0.01$, $\alpha_B = 0.01$, and $V_{DD} = 1\,\mathrm{V}$.

be increased, however this is limited by the transistor technology which has been selected. Thus advanced techniques are required which will build on these fundamentals.

2.5 Fully-Integrated Capacitors

One of the simplest methods of improving the performance of SC power converters is through improving the quality of the flying capacitors used. The power density is directly related to the capacitance density, as that gives a measure of the flying capacitance available per unit area. The other variable of importance when characterizing a flying capacitor is the voltage tolerance, as this will dictate how the capacitor can be used. The work presented in [11] compares the capacitance densities of Metal Oxide Metal (MOM), Metal Insulator Metal (MIM) and Metal Oxide Semiconductor (MOS) capacitors.

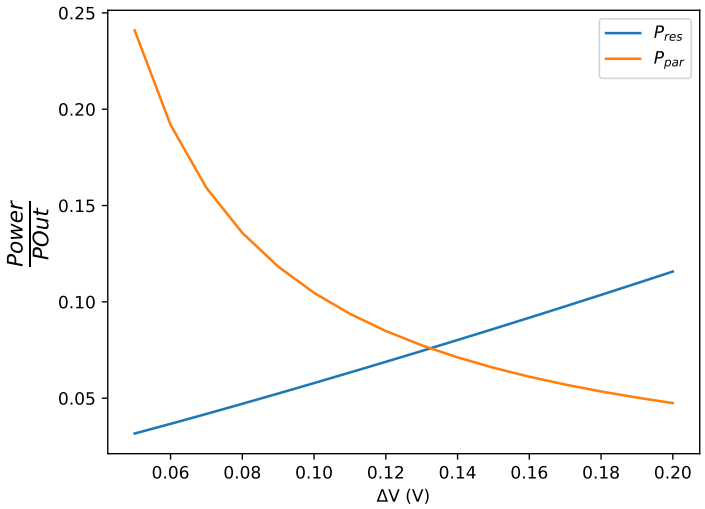


Figure 2.5: Loss ratios for the capacitive and resistive losses, as a fraction of the output power with $\alpha_T = 0.01$, $\alpha_B = 0.01$, and $V_{DD} = 1\,\mathrm{V}$.

2.5.1 MOM Capacitors

One of the most basic types of capacitors is the MOM capacitor which is formed between metal wires and insulated using the oxide, and thus does not require additional masks. The design of MOM capacitors can be understood using parallel plate theory, though many MOM capacitor designs involve interleaved digits, and are not well approximated by this theory. The rough relation is,

$$C = \frac{\epsilon A}{d}, \tag{2.21}$$

where A is the exposed surface area of the plate, d is the distance between plates, and ϵ is the dielectric constant of the material between the plates. As designers there is no control over the dielectric material in MOM capacitors, so the goal is to reduce the distance and increase the exposed area as much as possible. The minimum distance is going to depend on the minimum feature size of the technology which dictates rules like spacing for parallel wires.

The capacitance density will also be highly dependent on the number of metal layers and their thickness, where a larger number of thick metal layers will substantially increase the capacitance density per unit area, as MOM capacitors make efficient use of vertical space.

The voltage tolerance will depend on the breakdown of the insulator and will depend on the minimum feature size.

Some basic numbers for the voltage tolerance, and capacitance density of MOM capacitors were reported at 0.8 to 2.5 fF/μm^2, which were reported as functioning above 10V [12]. There has been work done on improving the density of MOM capacitors [13], in which several structures were examined and new ones were proposed.

The top and bottom plate parasitic capacitances of the MOM capacitor will depend on the design used. The contributors are the metal forming the perimeter of the structure, as well as the metal forming the bottom of the structure. However, the perimeter capacitances can likely be neglected for large structures, as the perimeter capacitances will scale with the square root of the capacitor area. The bottom of the MOM capacitor can be designed to either be a plate, or comprised of inter digitized fingers. Inter digitized fingers will yield both top and bottom plate parasitic capacitances, while a plate will shield one of the input terminals of the device, and create a parasitic capacitance on the other.

The parasitic capacitance associated with the bottom of the capacitor is going to be formed between the bottom metal layer, with the oxide between M0 and the conductive substrate forming the capacitor. The exact capacitance can be simulated using CAD tools which compute capacitances, and factor in the numerous metal and insulating layers such as ASITIC [14].

2.5.2 MIM Capacitors

An additional type of capacitor used is the MIM capacitor, in which the capacitor is formed between two metal layers, with insulator in between. This

means that the capacitance density of MIM capacitors is dependent on the electric permittivity of the insulator, as well as the spacing between layers. The parasitic capacitance is a function of the distance of the MIM capacitor to the ground layer of the substrate, as well as the electric permittivity of the insulating layer used, making it highly process dependent. From [11], MIM capacitors have very minimal leakage through the insulator in the 65 nm process, in addition, they are highly linear, and have a relatively high corner frequency. A capacitance density of $5\text{fF}/\mu\text{m}^2$ was reported with a voltage tolerance of 5.5V in STM's 65 nm CMOS process [12].

The parasitic capacitance formed by the MIM capacitor is going to be a result of the capacitance between the bottom plate and the substrate. This will result in a similar parasitic capacitance to that of a MOM capacitor, though the exact value will depend on what metal layer the bottom plate is on.

2.5.3 MOS Capacitors

Another type of integrated capacitor is the Metal Oxide Semiconductor (MOS) capacitors, which form a capacitor between a metal layer, gate oxide and the semiconductor channel. These capacitors have high densities, as the oxide of transistors is typically much thinner than the insulating layer in MOM capacitors. One of the issues associated with MOS capacitors is their traditionally high parasitic capacitance ratio, associated with the capacitance between the capacitor and the bulk of the substrate. Attempts have been made to significantly reduce this capacitance, enabling high efficiency's in combination with high power densities. Some capacitance densities are reported in Table 2.1, indicating the power density trends with technology nodes.

There are several ways to build MOS capacitors which depend on the technology modifications available. The most basic form of MOS capacitor is to use a PMOS transistor, wire the source and drain together, and connect the bulk of the transistor to a bias.

Table 2.1: Capacitance densities of different MOSFET technologies. Values taken from [15, 12] are for C_{ox}, meaning they may slightly overestimate the net capacitance density.

Technology (μm)	Capacitance Density (fF/μm^2)	Max Voltage (V)
0.8	1.9 [15]	-
0.5	2.03 [12]	5 [12]
0.35	4.5 [15]	-
0.25	3.04 [12]	2.5 [12]
0.18	8.5 [15]	-
0.065	11 [11]	1 [11]
0.045	25 [15]	-

The work in [16] features the use of a PMOS capacitor in 65nm CMOS, in which the bulk is wired to a high impedance bias. This results in the parasitic capacitance being formed by the series combination of the channel coupling to the bulk, and the capacitance between the bulk and the substrate. The reported parasitic capacitance ratio was 1.2%, for the bottom plate, while no top plate capacitance was reported.

A depletion mode p-type capacitor was tested where the surrounding deep n-well was biased in order to reduce its parasitic capacitance [17]. This results in a parasitic capacitance being formed between the p-well and the deep n-well, where the parasitic capacitance is a function of the bias voltage and the bottom plate voltage.

The depletion mode p-type capacitor can be modified to make the bias high-impedance [18], which results in the parasitic capacitance being formed between the series combination of the p-well, deep n-well interface, and the deep n-well p-substrate interface. The α_B was reported as being less than 1%, with no reported values for α_T.

Accumulation mode NMOS devices can also be used, which are simple to implement and make use of the existing process masks for PMOS transistors. A diagram of the corresponding flying capacitor is in Figure 2.6. The result is that the only parasitic capacitance formed by the structure is between the

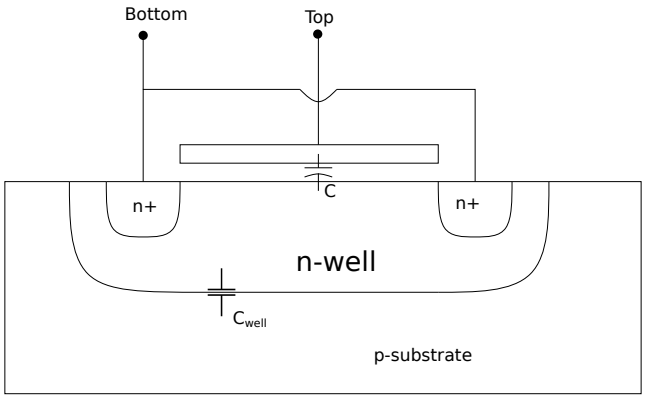


Figure 2.6: Accumulation mode NMOS flying capacitor

well and the substrate itself. The reported α_B was 1.2%, and the reported α_T was 1.1%.

2.6 Transistor Selection

One of the important factors in fully-integrated SCPC is the use of transistors in place of the diodes frequently present at higher voltages. Transistors can be used to eliminate the forward bias voltage drop typically associated with charge transfers, increasing the efficiency at low supply voltages. Transistors require careful control in most SC topologies, ensuring that they do not short circuit power or exceed any of their breakdown voltages. The on resistance of the transistors used will determine the switching frequency (f_{SW}) of the converter, as there is an RC time constant formed between the transistor and the flying capacitor. Ideally, integrated converters would be operating at as high a frequency as possible in order to maximize their respective power outputs.

The equation for the on resistance of an NMOS transistor is,

$$R_{ON} = \frac{L}{W\mu_n C_{ox}(V_{GS} - V_t)} \tag{2.22}$$

where L is the channel length, W is the channel width, C_{ox} is the capacitance per unit area of the oxide, μ_n is the carrier mobility of the transistor, V_{GS} is

the gate to source voltage drop, and V_t is the threshold voltage. It should be noted that in a specific technology, there is a minimum L, and a maximum V_{GS} before the safe voltage levels of the transistor are reached. The only solution left available to the designer, is to then increase W, reducing the resistance.

The consequence of increasing the width of the transistor is the resulting increase in the gate capacitance, C_G, and the drain to bulk capacitance C_{DB}. The expression for C_G in the triode region is,

$$C_G = C_{ox} W L, \tag{2.23}$$

while the capacitance between the drain and the source is largely a result of the

$$C_{db} = A_d C_{jd}, \tag{2.24}$$

where A_d is the area of the drain terminal, and C_{jd} is the capacitance density of the drain junction. The exact values associated with C_{db} are highly process dependent, however the area of the drain is going to be directly proportional to W, especially for transistors many times wide than long. These parasitic capacitances will then decrease the efficiency of the design, creating a trade-off between operating frequency and efficiency. This trade-off between capacitance and on-resistance also exists for the PMOS transistors, which have a similar on resistance of,

$$R_{ON} = \frac{L}{W \mu_p C_{ox} (V_{SG} - |V_t|)} \tag{2.25}$$

where μ_p is the carrier mobility of the PMOS transistor.

The final point of consideration for a given CMOS technology is the voltage tolerance of the transistors. Typically, the technology will have a maximum voltage tolerance between its three terminals, limiting the applied voltage to the gate, as well as the drain to bulk voltage.

2.6.1 Deep n-Well NMOS

One critical CMOS technology that is important for the majority of the converter topologies is the deep n-well NMOS transistor. This isolates the bulk

of the NMOS, which is not usually the case for NMOS, as they typically have a bulk connection directly to the substrate ground. This will allow designers to use NMOS at terminals where the source or drain are higher than V_{DD}.

2.7 Circuit Level Techniques

One of the additional categories under which to improve SC power converters are the broadly applicable circuit level techniques which work for many integrated SC power converters.

2.7.1 Time Interleaved Converters

In order to reduce the output voltage ripple, in addition to reducing the variance in the input current, a technique referred to as time interleaving can be used. The technique functions by taking a single SC converter and splitting the area associated with the converter into several sub blocks, referred to as "cores". Each core is comprised of flying capacitors with their own drivers and unique clock. The individual cores operate in a tightly synchronized manner, such that none of these cores deliver power to the output at the same time. This has the effect of reducing the output ripple, as the current is delivered more evenly. This also has the effect of reducing the input ripple current, reducing demands on the supply voltage. The work done in [19], [20] for example, successfully use time interleaving to reduce the output ripple substantially.

The resulting decrease in output capacitor size (or complete elimination of it) is extremely useful for fully-integrated SC converters, as the output capacitor is effectively wasted area.

The distribution and clocking of the individual cores is usually accomplished using a clock division scheme, in which there is a global clock operating at many times the frequency of the individual cores. The output of the clock divider is then distributed to the many cores, ensuring that they are all out of phase with each other.

2.7.2 Charge Reuse

In order to reduce the amount of capacitive losses in a system and increase the maximum efficiency, charge reuse techniques can be employed. Charge reuse functions by taking any parasitic capacitance in the system which is periodically charged and discharged and saving the charge when the capacitance discharges to pre-charge it on the next rising transition.

2.7.2.1 Bottom Plate Equalization

The simplest form of charge reuse is bottom plate equalization (BPE), in which the two cores which are 180° out of phase have their bottom plates equalized between their charge and discharge phases. A voltage doubler schematic implementing BPE can be seen in Figure 2.7, with a respective timing diagram in Figure 2.8. The two primary clocks must be disabled before ϕ_3 can be enabled in order to prevent short circuit currents. BPE saves 50% of the power that would have been wasted charging the bottom plate, and close to 50% of the top plate.

Several SC power converters have been simulated or tested which use BPE, all of which indicate an improvement in performance [21], [22], [9].

2.7.2.2 Generic n level charge reuse

A generic level of charge reuse can be implemented, in which instead of 1-level of equalization as in BPE, n-levels of charge reuse can be implemented. As there is not any existing model which completely derives the impact of charge reuse on the system, one can be developed.

Generic n-level charge reuse was implemented in both [23] and [24], and while the effect on bottom plate parasitic capacitance reduction was reported as,

$$P_{BP} = \frac{P_{BP,regular}}{n+1}. \tag{2.26}$$

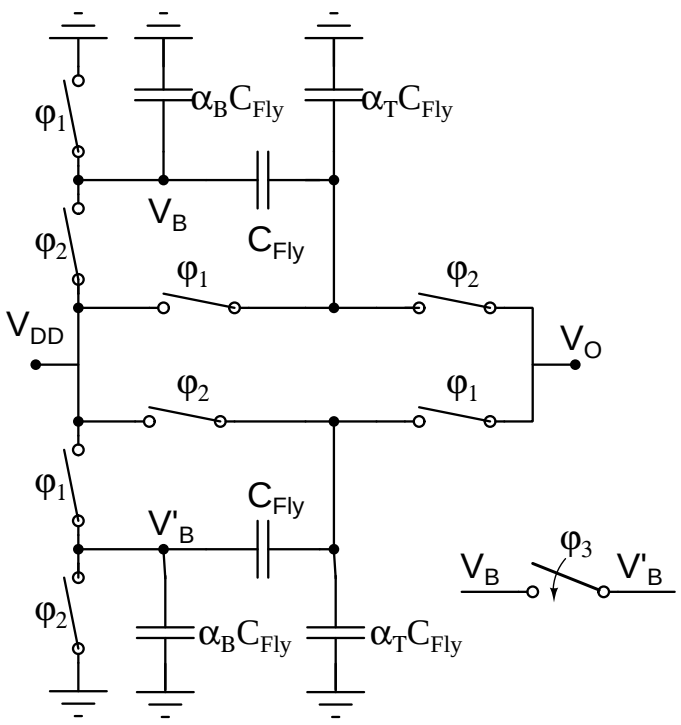


Figure 2.7: Voltage double with ideal switches and BPE

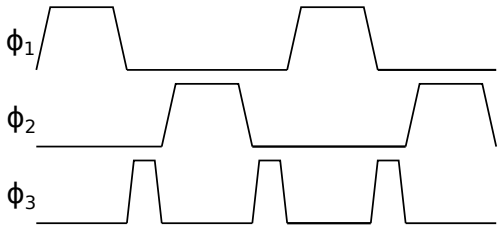


Figure 2.8: Voltage doubler with ideal switches and BPE

Additionally, [25] defines the amount of energy required to charge a load capacitor as,

$$E_{SW} = \frac{C_L V_{SW}^2}{n+1}, \tag{2.27}$$

which agrees with the formulation in [23].

2.7.2.3 Transistor Gate Charge Reuse

An analysis was performed on the results of using charge reuse to minimize the gate driving losses of an SCPC [26]. The results indicate that the technique is likely suited for a small subset of applications and are not nearly as broadly applicable as charge reuse on other internal nodes.

2.7.3 Soft Charging

Soft charging typically refers to a method in which the flying capacitors are charged gradually, with a progressively increasing voltage drop, rather than an rapid voltage drop, as with standard SC converters. The proposed design in [27], implements soft charging with a current source driven output stage, to be implemented for inductive loads. As a result of the reduction in root mean squared current, the power losses on the switches are found to decrease substantially. This method of soft charging was then implemented using off-chip inductors and a substantial decrease in output resistance was obtained [28]. Finally, the inductor based SC design was improved on by splitting the discharge phases in an SC converter strategically so as to further minimize the RMS current [29], though an off-chip inductor is still required.

Soft charging techniques can be extended to more traditional SC converters with at least 1 intermediary voltage domain [18], though the effects are not nearly as pronounced as those in [27]. The operation works by splitting the intermediary voltage domain into sub-levels levels to improve the efficiency. Consider a 2 stage doubler in the buck configuration, there will be 3 voltage domains in the converter, spaced evenly between V_{IN} and gnd. The second

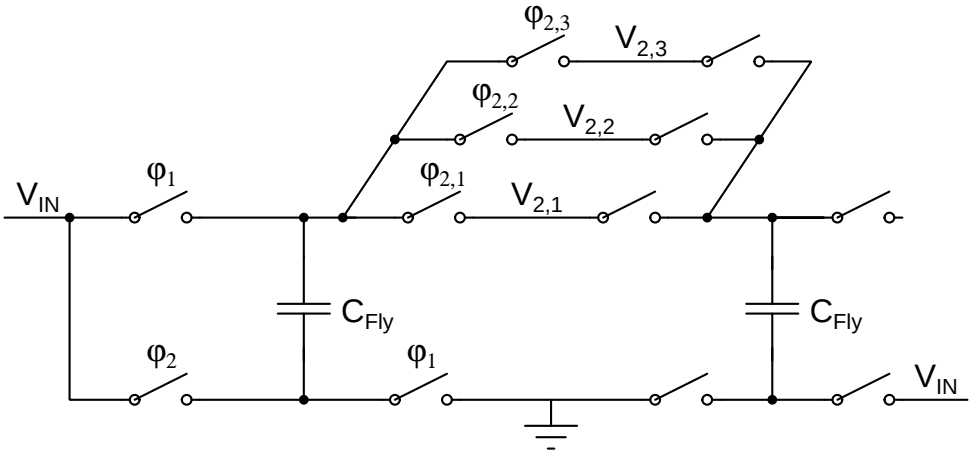


Figure 2.9: Two Stage Doubler Charge Pump with three soft charging intermediary levels

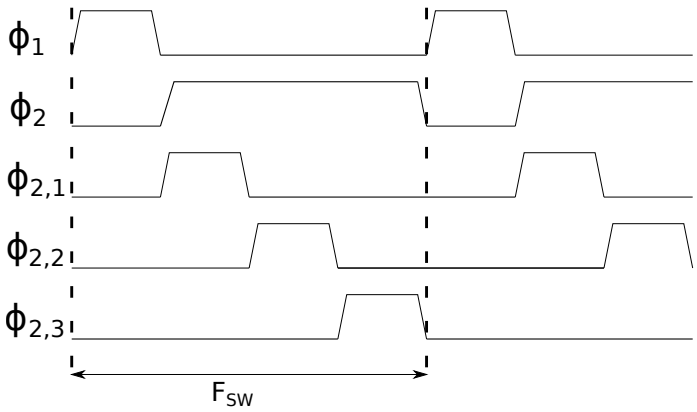


Figure 2.10: Timing diagram for an S=3 multiphase charge pump

voltage domain (V_2) is related to the output through the relation,

$$V_2 = \frac{2V_{IN}}{2} - \Delta V/2, \tag{2.28}$$

where $\Delta V = \frac{V_{IN}}{3} - V_{OUT}$, assuming the first and second stage of the charge pump have equally sized flying capacitors.

Soft charging works by sub-dividing any internal voltage domain into (S) unique internal levels, this excludes the output and input voltage, as those are fixed. For example, Figure 2.9 illustrates a system where, V_2 of the 3:1 doubler is divided into S sub domains - $V_{2,k}$, where k ranges from 1 to S. The figure does not have some of the switch timings listed, as a result of the complex time interleaving involved in the structure. There would be a minimum of 8 cores associated with this design, where one core is simultaneously always connecting to each voltage domain from the first and second stage. A timing diagram corresponding to Figure 2.9, is in Figure 2.10. The expression for the voltage on the sub-domains is approximately,

$$V_{2,k} \approx 2V_{IN} - \frac{k\Delta V}{2S}. \tag{2.29}$$

This results in the transfer of charge to the internal node occurring over S unique intervals. This results in a reduction in I_{RMS} by a factor of S, reducing the resistive losses for the internal charge transfer by a factor of S. The reduction in resistive losses of the entire 3:1 converter can be expressed as,

$$A = \frac{1 + \frac{1}{S}}{2}, \tag{2.30}$$

where A is the relative resistive losses. Comparatively, the expression for a generic N number of stages is,

$$A = \frac{1 + \frac{N-1}{S}}{N}, \tag{2.31}$$

indicating that larger values of N receive larger benefits from multiphase soft charging. This reduction in resistive losses results in higher conversion efficiencies, as well as a reduction in input ripple.

2.7.4 Variable Conversion Ratio

There is substantial interest in utilizing variable conversion ratio SC converters, as varying input voltages can occur, and modifying the conversion ratio to maintain efficient power transfer is important.

- The work presented in [30], successfully presents a circuit topology that has a variable conversion ratio of 4, 5, 6, 7, and 8x.
- The work presented in [31], demonstrates a multi-output SC converter with boost and buck configurations, while re-using the flying capacitors for better area efficiency.
- [32] features a simultaneous 3:2 and 3:1 ratio converter with multiple output voltages using time interleaving techniques.
- [33] uses a charge recycling method to regulate the amount of charge stored on the flying capacitors and should allow for a voltage range between 1.5x and 3x at the expense of 2 times the flying capacitance area.
- [34] employ a 3:2, 2:1 re-configurable converter with switch boosting, and discrete capacitors, though the design could be modified to support a 3:1 conversion ratio as well.
- [35] uses 6 discrete flying capacitors and re-configures them to get conversion ratios of between 4:1 and 1:2, with excellent efficiency across the range.
- [36] uses high density MIM capacitors in combination with 22 nm silicon to achieve high power densities with re-configurable ratios of 1:1, 5:4, 3:2 and 1:2.
- [37] uses a re-configurable step down configuration from 5:1 to 2:1, and analyzes the trade offs and transistor sizing for the design used, in addition to providing an efficiency model.
- [38] features re-configurable ratios of 3:2, 4:3, 2:1, 3:1, 4:1, in addition to a control system which dynamically selects the ratio to yield the optimal efficiency.
- [39] uses re-configurable ratios of 1, 3:2, 2:1 and 3:1, in combination with ferro-electric capacitors for their reduced parasitic capacitance.

2.8 SC Modelling

There is minimal difference between the modelling of fully integrated SC converters and those with off-chip capacitors. One of the major differences is that off-chip capacitors typically have much lower parasitic capacitance values, allowing for a simplification of the models and equations used. Most models used assume the capacitors used are linear, and that the transistors can be approximated as switches with a constant on resistance.

The net system model of the SC power converter is typically characterized as a transformer with an output resistance, where the conversion ratio is controlled by the transformer [40]. Additionally, the output resistance can be characterized by a slow switching limit (SSL), in which the output resistance is almost exclusively a function of the flying capacitance and the switching frequency [41]. The Fast Switching Limit (FSL) refers to the high frequency limit, where the output resistance is instead limited by the on resistance of the transistors. The work in [42] successfully models the simulated performance using a high dimension matrix, no single expression for the FSL is provided. The power flow in multi-stage SC converters is important for the design and optimization of the number of stages, and has been modelled in the literature, though the analysis excluded parasitic capacitors [43].

Chapter 3

Charge Reuse Analysis and Trade-offs

Seeing as it is a technique which can substantially improve the efficiency and performance of SC power converters. Unfortunately, there has been little quantitative research done on modelling the exact impacts and design trade-offs associated with charge reuse. The work in [23] provides a breakdown of the qualitative effects of charge reuse, as well as some general models, but do not provide explicit derivations the exact impact of charge reuse on the system.

The exact impact of charge reuse on efficiency should be investigated, in addition to the time required each cycle for charge reuse. The subsequent analysis is performed assuming the system has reached steady state.

3.1 Steady State Analysis

An example of n level charge reuse is shown in Figure 3.1 which implements an $n = 3$ level charge reuse. The corresponding transient behaviour of V_C and the corresponding clock signals is shown in Figure 3.2, where the change in voltage on the load capacitor can be seen. The power savings associated with

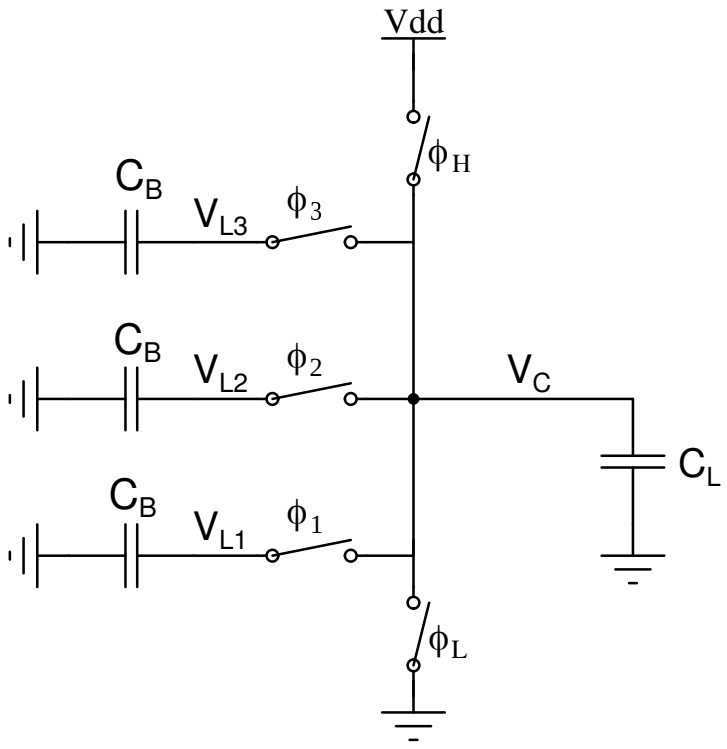


Figure 3.1: Charge reuse circuit with $n = 3$ levels, used to charge and discharge a load capacitance (C_L). The bank capacitors (C_B) can be considered many times larger than C_L to simplify the analysis.

this technique are well captured by the equation,

$$E_{SW} = \frac{C_L V_{DD}^2}{n+1}, \tag{3.1}$$

[25], which indicates a substantial reduction compared to the typical $n = 0$ case. The voltages stored on the bank capacitors C_B are equally spaced from V_{DD} to 0,

$$V_{Lh} = \frac{hV_{DD}}{n}, \tag{3.2}$$

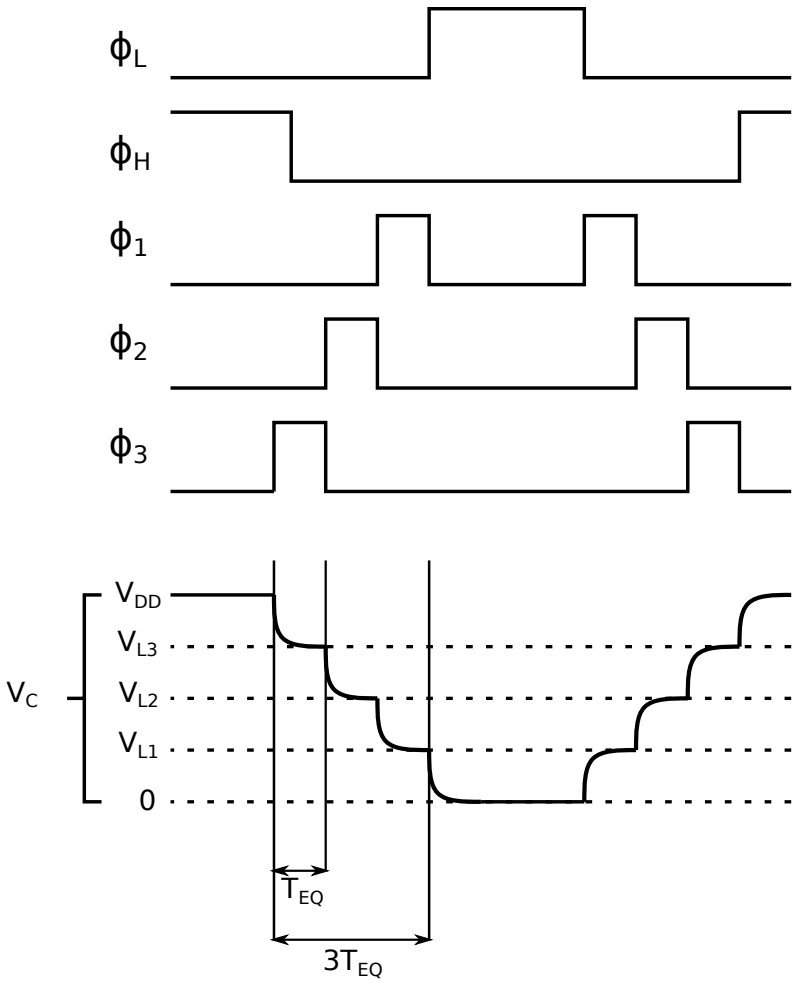


Figure 3.2: Timing diagram of V_C with respect to time

where h is the respective level from 1 to n. This technique can be applied directly to any internal node of the converter. One of the simplest nodes to use is the bottom plate of the flying capacitor.

3.2 Bottom Plate Charge Reuse

Now the equations can be explored in the context of the SC power converter cell in the boost configuration, where charge reuse is used to save power on the bottom plate. Consider the converter as it transitions from the first phase, where the bottom plate is grounded, and the top plate is connected to V_{DD}. Next, the converter begins its charge reuse process, driving the bottom plate from 0 to V_{Ln}, where

$$V_{Ln} = \frac{nV_{DD}}{n+1}, \tag{3.3}$$

however the voltage at the top node is not known. In order to calculate V_T, the change in V_T can be acquired using by performing a nodal analysis at V_T in the frequency domain, where

$$s\alpha_T C_{Fly} V_T + sC_{Fly}(V_T - V_B) = 0, \tag{3.4}$$

which can be re-written in the time domain to describe the change in top plate voltage relative to the bottom plate,

$$\Delta V_T = \frac{\Delta V_B}{1+\alpha_T}. \tag{3.5}$$

This indicates that the final voltage on V_T during the rising transition is,

$$V_{Tn} = V_{DD} + \Delta V_T = V_{DD} + \frac{nV_{DD}}{(n+1)(1+\alpha_T)}. \tag{3.6}$$

Now the transition to the next phase can be performed, as both the top and bottom plate nodal voltages are known. The amount of charge delivered to

the output can be calculated as,

$$\begin{aligned}
Q_{OUT} &= C_{Fly}(V_{Tn} - V_{T2} + V_{B2} - V_{Bn}) + \alpha_T C_{Fly}(V_{Tn} - V_{T2}), \\
&= C_{Fly}(V_{DD} + \tfrac{nV_{DD}}{(n+1)(1+\alpha_T)} - 2V_{DD} + V_{DD} - \tfrac{nV_{DD}}{n+1}) + \alpha_T C_{Fly}(V_{Tn} - V_{T2}) \\
&= C_{Fly}(\tfrac{nV_{DD}}{(n+1)(1+\alpha_T)} + \Delta V - \tfrac{nV_{DD}}{n+1}) + \alpha_T C_{Fly}\left(\tfrac{nV_{DD}}{(n+1)(1+\alpha_T)} - V_{DD} + \Delta V\right) \\
&= C_{Fly}\Delta V - \alpha_T C_{Fly}(V_{DD} - \Delta V),
\end{aligned} \tag{3.7}$$

which has no dependence on the amount of charge reuse that has occurred on the bottom plate, indicating that bottom plate equalization has no direct impact on the output current or equivalent resistance. The equation can be further verified by comparing it to the output current formulation in [44], which describes the output current for an N stage Dickson converter,

$$I_{OUT} = \frac{f_{SW} C_{Fly}(1+\alpha_T)}{N}\left(\left(\frac{N}{1+\alpha_T} + 1\right) V_{IN} - V_{OUT}\right), \tag{3.8}$$

where N is the number of stages. The equation can be re-purposed for a single stage by setting $N = 1$, and simplifying,

$$\begin{aligned}
I_{OUT} &= f_{SW} C_{Fly}(1+\alpha_T)\left(\frac{2+\alpha_T}{1+\alpha_T} V_{IN} - V_{OUT}\right) \\
&= f_{SW} C_{Fly}(1+\alpha_T)\left(\frac{2+\alpha_T}{1+\alpha_T} V_{DD} - 2V_{DD} + \Delta V\right) \\
&= f_{SW} C_{Fly}(1+\alpha_T)\left(\Delta V - V_{DD}\frac{\alpha_T}{1+\alpha_T}\right) \\
&= f_{SW} C_{Fly}(1+\alpha_T)\left(\Delta V - V_{DD}\frac{\alpha_T}{1+\alpha_T}\right) \\
&= f_{SW} C_{Fly}\left(\Delta V - \alpha_T(V_{DD} - \Delta V)\right),
\end{aligned} \tag{3.9}$$

which is equivalent to the output current for the n charge reuse case, as $I_{OUT} = Q_{OUT} f_{SW}$. Next, the amount of charge drawn from the input can be calculated in a similar manner,

$$\begin{aligned}
Q_{IN} &= C_{Fly}(V_{Tn} - V_{T2} + V_{B2} - V_{Bn}) + \alpha_B C_{Fly}(V_{DD} - V_{Bn}), \\
&= C_{Fly}\left(\Delta V - \frac{n\alpha_T}{(n+1)(1+\alpha_T)}\right) + \alpha_B C_{Fly}\frac{V_{DD}}{n+1} \\
&= C_{Fly}\left(\Delta V\right) + C_{Fly}\left(\alpha_B - \frac{n\alpha_T}{1+\alpha_T}\right)\frac{V_{DD}}{n+1},
\end{aligned} \tag{3.10}$$

which has a dependence on the quantity of charge reuse that has occurred. The net impact of bottom plate equalization can be summarized as a change in α_B,

$$\alpha_B^* = \frac{1}{n+1}\left(\alpha_B - \frac{n\alpha_T}{\alpha_T+1}\right) \tag{3.11}$$

where α_B^* is the new effective bottom plate parasitic capacitance ratio. This new bottom plate parasitic capacitance ratio can then be factored into the existing equations for efficiency, output resistance, and so on in order to generate accurate models without redoing existing calculations.

The new peak efficiency for a single stage is,

$$\hat{\eta} = 1 - \frac{2}{\sqrt{\frac{(2+\alpha_T)^2}{\alpha_B^*+\alpha_T+\alpha_T\alpha_B^*}+1}+1}, \tag{3.12}$$

using the efficiency calculation formulated in [9].

3.3 Top Plate Charge Reuse

Next, the impact of performing charge reuse on the top plate should be investigated, this time starting from the nodal equation on the bottom plate,

$$s\alpha_B C_{Fly} V_B + sC_{Fly}(V_B - V_T) = 0, \tag{3.13}$$

which can be re-arranged and converted to the time domain to yield,

$$\frac{dV_B}{dt} = \frac{dV_T}{dt}\frac{1}{1+\alpha_B}. \tag{3.14}$$

Next the voltage on the top plate at the last step of charge reuse can be calculated,

$$V_{Tn} = V_{Ln} = V_{DD} + \frac{n(V_{OUT} - V_{DD})}{n+1}, \tag{3.15}$$

the final bottom plate voltage can then be calculated as,

$$V_{Bn} = \frac{n(V_{OUT} - V_{DD})}{(n+1)(1+\alpha_B)}. \tag{3.16}$$

Using the top and bottom plate voltages, the output charge can the be calculated,

$$\begin{aligned} Q_{OUT} &= C_{Fly}(V_{Tn} - V_{OUT} + V_{B2} - V_{Bn}) + \alpha_T C_{Fly}\left(V_{Tn} - V_{OUT}\right) \\ &= C_{Fly}\left(\tfrac{n(V_{OUT}-V_{DD})}{n+1} - V_{OUT} + 2V_{DD} - \tfrac{n(V_{OUT}-V_{DD})}{(n+1)(1+\alpha_B)}\right) \\ &+ \alpha_T C_{Fly}\left(V_{Tn} - V_{OUT}\right) \\ &= C_{Fly}\left(\tfrac{\alpha_B n(V_{OUT}-V_{DD})}{(n+1)(1+\alpha_B)} + \Delta V\right) \\ &+ \alpha_T C_{Fly}\left(\tfrac{n(V_{OUT}-V_{DD})}{n+1} - V_{DD} + \Delta V\right) \\ &= C_{Fly}\left(\tfrac{\alpha_B n(V_{OUT}-V_{DD})}{(n+1)(1+\alpha_B)} + \Delta V\right) + \alpha_T C_{Fly}\tfrac{V_{DD}-\Delta V}{n+1} \\ &= C_{Fly}\Delta V + \left(\alpha_T - \frac{n\alpha_B}{1+\alpha_B}\right) C_{Fly}\tfrac{V_{DD}-\Delta V}{n+1} \end{aligned} \tag{3.17}$$

which indicates that the effect of top plate equalization is highly symmetric to bottom plate equalization, where the effective top plate parasitic capacitance is,

$$\alpha_T^* = \frac{1}{n+1}\left(\alpha_T - \frac{n\alpha_B}{1+\alpha_B}\right). \tag{3.18}$$

The result is that charge reuse has a relatively simple effect on the system, transforming either α_B or α_T depending on which node it is used on.

3.3.1 Model Verification

In order to verify the accuracy of the calculations performed, both top and bottom plate equalization were tested for the single stage voltage doubler. The charge reuse was implemented using a capacitor bank with capacitors over 100 times the size of the parasitic capacitor to guarantee accuracy. All the capacitors used in the simulation are linear and ideal, and full equalization is used for all charge transfers. The input voltage is held constant at 1 V, the output voltage is generated with an ideal voltage source, and all simulation data is acquired at steady state.

Four simulations were run for both top plate and bottom plate charge reuse, where the values of n, and α_B are varied. The simulations are then

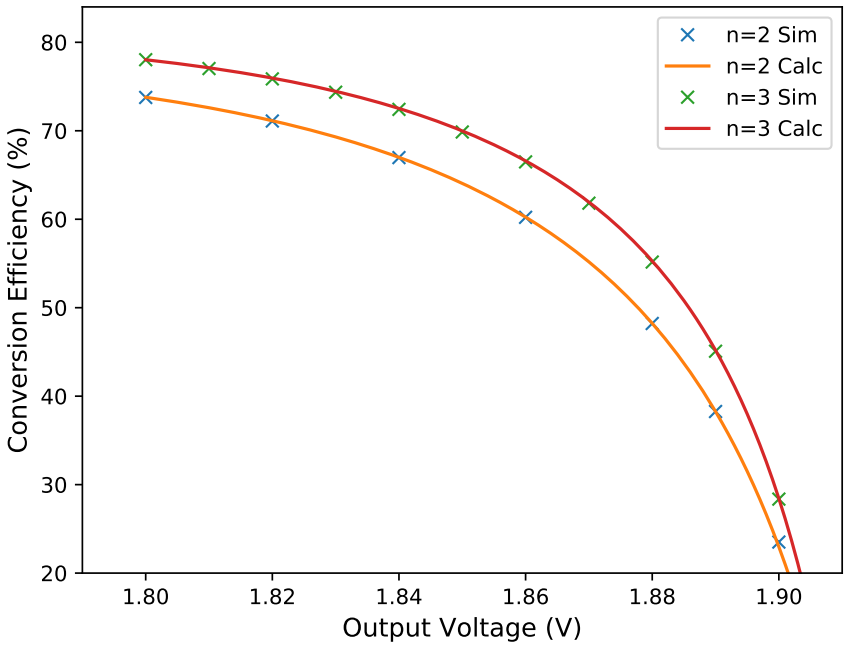


Figure 3.3: Power conversion efficiency for a single stage voltage doubler with BPE, and an $\alpha_B = \alpha_T = 0.1$.

compared to the efficiency calculation in [44], substituting in α_B^* or α_T^*. The results of implementing charge reuse on the bottom plate can be seen in Figure 3.4 and Figure 3.3, which indicate that the calculated efficiency matches the simulated. Similarly, the top plate charge reuse results are in Figure 3.6, and Figure 3.5, which also match the calculations.

An additional set of simulations were run in order to verify the accuracy of the α_B^* transformation for the multi-stage voltage doubler. A 3-stage voltage doubler was tested, with ideal switches and capacitances, and at steady state. The resulting comparison between the calculated and simulated results can be seen in Figure 3.7.

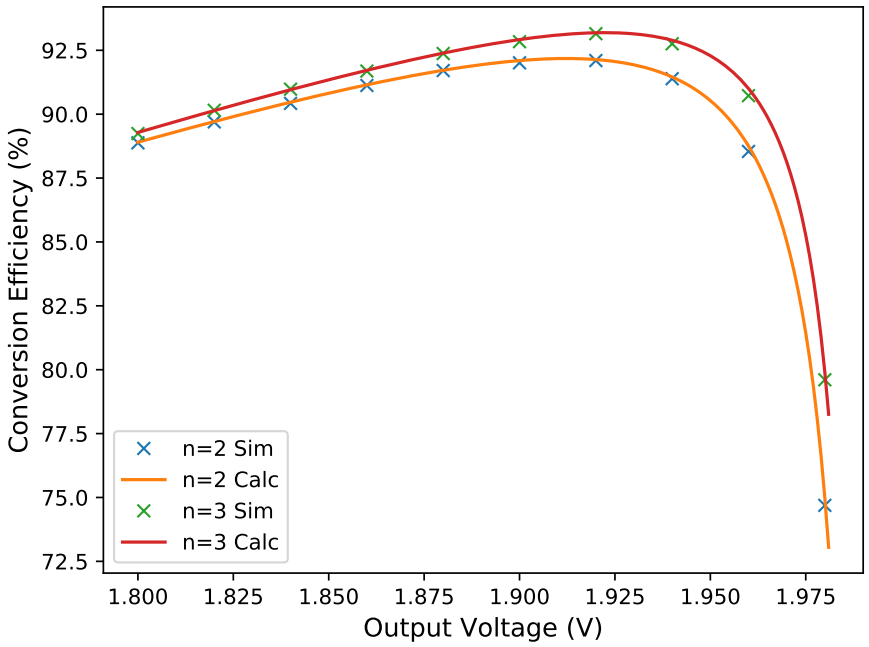


Figure 3.4: Power conversion efficiency for a single stage voltage doubler with BPE, and an $\alpha_B = \alpha_T = 0.01$.

3.4 Transient Analysis

There are two most major costs to implementing charge reuse, the first is the area associated with any external capacitor and control circuitry, and the second is the time required to actually recover the charges. Any time spent charging or discharging the parasitic capacitor is time that could be spent delivering power, and thus should be kept to a minimum. Consider the example timing diagram in Figure 3.2, which includes $n = 3$ levels of charge reuse, each with time T_{EQ} dedicated to them. How should the designer select this time? How large should the transistors used to equalize the parasitic capacitor to V_{Lh} be?

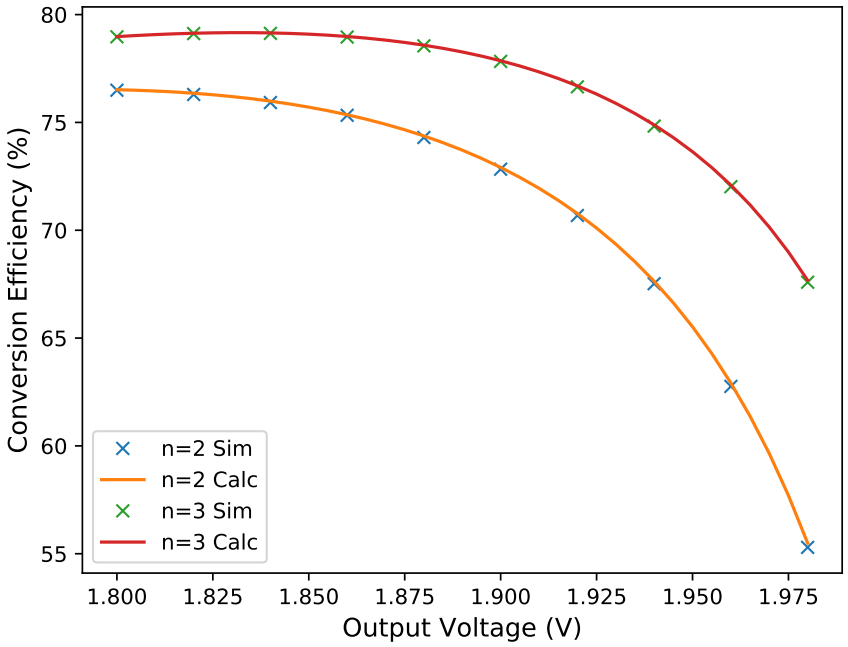


Figure 3.5: Power conversion efficiency for a single stage voltage doubler with TPE, and an $\alpha_B = \alpha_T = 0.1$.

The analysis in [25] provides an excellent starting place, which can be adapted to the charging and discharging of the parasitic capacitors. There has been analysis done to calculate the minimum energy savings as a function of the time for a generic load capacitor,

$$E_{SW} = \frac{3}{2}\sqrt[3]{\frac{4m\rho}{T}}C_L V_{DD}^2, \tag{3.19}$$

where C_L is the respective load capacitance, $T = nT_{EQ}$, m is the number of RC time constant equal to the equalization transistor (R_{EQ}) and C_L, and ρ is a device parameter relating the on resistance of the equalization transistors, and their respective gate capacitance (C_{EQ}),

$$\rho = R_{EQ}C_{EQ}. \tag{3.20}$$

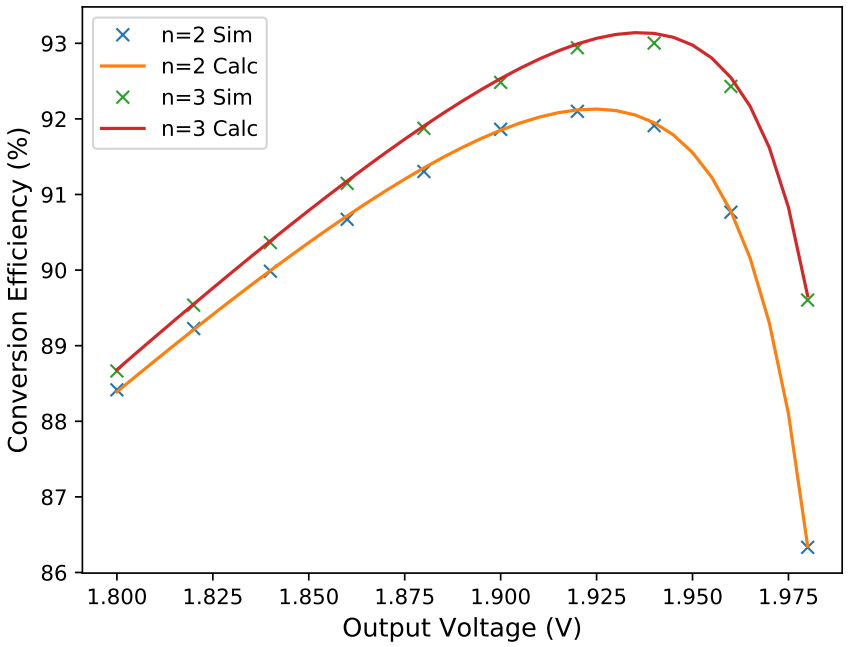


Figure 3.6: Power conversion efficiency for a single stage voltage doubler with TPE, and an $\alpha_B = \alpha_T = 0.01$.

The optimal number of charge reuse stages n was also defined,

$$n = \sqrt[3]{\frac{T}{4m\rho}} - 1. \tag{3.21}$$

The results indicate that the amount that the parasitic capacitance can be reduced is proportional to T^3, indicating that high levels of n are unrealistic in high power systems.

3.4.1 Incomplete Charge Transfer

One highly relevant point in the prior analysis did not factor in was the impact of the incomplete charge transfer resulting from a small value of τ. Figure 3.1 still pertains to the following $n = 3$ case of incomplete charge reuse, and the

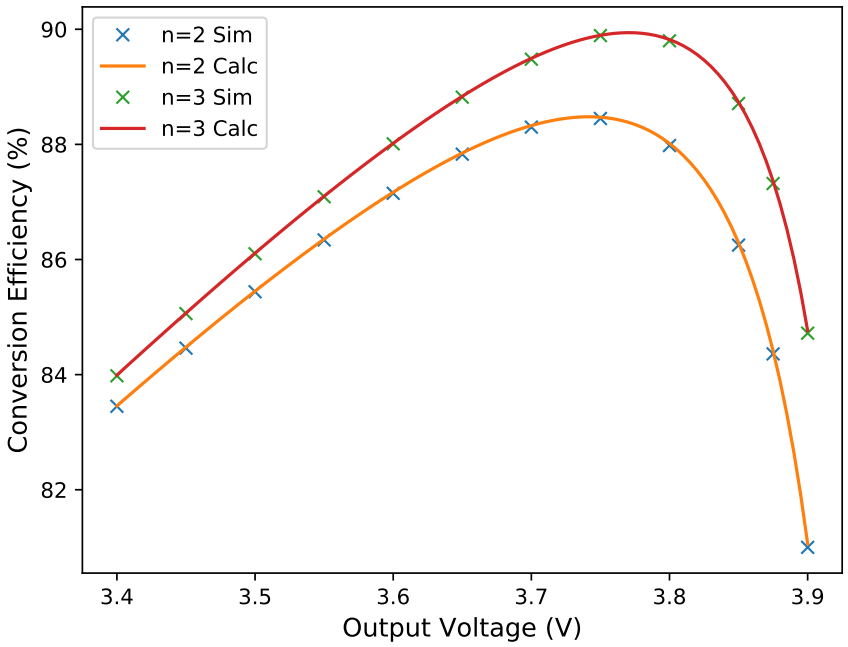


Figure 3.7: Power conversion efficiency for a three stage voltage doubler with TPE, and an $\alpha_B = \alpha_T = 0.1$.

variables used in the analysis reflect this. The analysis operates under the following assumptions,

- The capacitances involved are linear with respect to their stored voltage.
- The switches are all non-overlapping, preventing short circuit currents.
- The analysis is performed at steady state.
- The bank capacitors are sufficiently large relative to the load capacitance (C_L), that they do not contribute to the RC time constant or steady state voltages.
- Each switch is turned on and allows C_B to equalize with C_L for the same period of time (T_{EQ}).
- The series resistance of each individual equalization switch is R_{EQ}.

Under these assumptions the resulting fraction of charge transferred can be referred to as A where,

$$A = 1 - \exp\left(\frac{-T_{EQ}}{R_{EQ}C_L}\right), \tag{3.22}$$

Next, the voltages on the falling transition can be considered,

$$V_h = V_{h+1}(1 - A) + AV_{Lh}, \tag{3.23}$$

where V_h is the voltage on the parasitic capacitor before the next equalization step, where h indicates the equalization step, from n to 1. The voltages on the rising transition are,

$$V'_h = V'_{h-1}(1 - A) + AV_{Lh}, \tag{3.24}$$

which represent the voltage on the parasitic capacitor at the end of each equalization step. An illustration of the voltage transition is presented in Figure 3.8 for an $n = 3$ case, with V_h and V'_h labeled. The indexes V_0 and V_{n+1} indicate 0 and V_{DD}, respectively. Now a matrix expression of the voltages on the falling transition can be constructed, where

$$\begin{bmatrix} V_n \\ V_{n-1} \\ \vdots \\ V_2 \\ V_1 \end{bmatrix} = \begin{bmatrix} A & 0 & \dots & 0 & 0 \\ A(1-A) & A & \dots & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ A(1-A)^{n-2} & A(1-A)^{n-3} & \dots & A & 0 \\ A(1-A)^{n-1} & A(1-A)^{n-2} & \dots & A(1-A) & A \end{bmatrix} \begin{bmatrix} V_{Ln} \\ V_{Ln-1} \\ \vdots \\ V_{L2} \\ V_{L1} \end{bmatrix} + V_{DD} \begin{bmatrix} (1-A) \\ (1-A)^2 \\ \vdots \\ (1-A)^{n-1} \\ (1-A)^n \end{bmatrix}. \tag{3.25}$$

The amount of charge delivered to each voltage level on the falling transition can be calculated as,

$$Q_h = C\left(V_{h+1} - V_h\right), \tag{3.26}$$

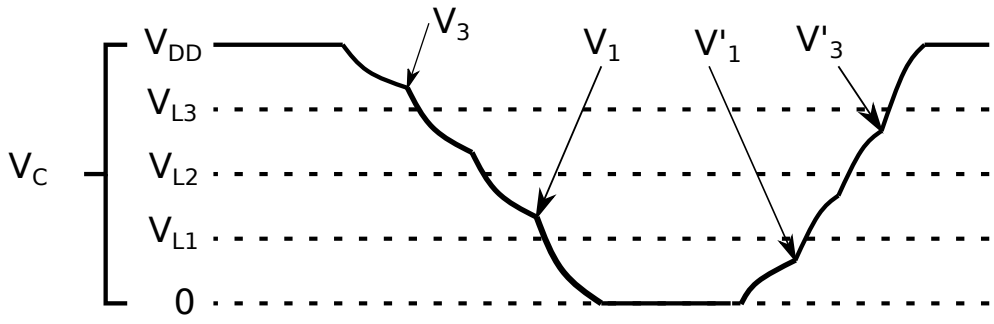


Figure 3.8: Charge reuse with incomplete charge transfer and transition voltages labeled.

which works out to,

$$\begin{bmatrix} Q_n \\ Q_{n-1} \\ \vdots \\ Q_2 \\ Q_1 \end{bmatrix} = \begin{bmatrix} -A & 0 & \dots & 0 & 0 \\ A^2 & -A & \dots & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ A^2(1-A)^{n-3} & A^2(1-A)^{n-4} & \dots & -A & 0 \\ A^2(1-A)^{n-2} & A^2(1-A)^{n-3} & \dots & A^2 & -A \end{bmatrix} \begin{bmatrix} V_{Ln} \\ V_{Ln-1} \\ \vdots \\ V_{L2} \\ V_{L1} \end{bmatrix} C + CV_{DD} \begin{bmatrix} A \\ A(1-A) \\ \vdots \\ A(1-A)^{n-2} \\ A(1-A)^{n-1} \end{bmatrix}. \tag{3.27}$$

The expression for the voltages during the rising transition can be constructed as,

$$\begin{bmatrix} V'_n \\ V'_{n-1} \\ \vdots \\ V'_2 \\ V'_1 \end{bmatrix} = \begin{bmatrix} A & A(1-A) & \dots & A(1-A)^{n-2} & A(1-A)^{n-1} \\ 0 & A & \dots & A(1-A)^{n-3} & A(1-A)^{n-2} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \dots & A & A(1-A) \\ 0 & 0 & \dots & 0 & A \end{bmatrix} \begin{bmatrix} V_{Ln} \\ V_{Ln-1} \\ \vdots \\ V_{L2} \\ V_{L1} \end{bmatrix}. \tag{3.28}$$

while the equation for the charge is,

$$\begin{bmatrix} Q'_n \\ Q'_{n-1} \\ \vdots \\ Q'_2 \\ Q'_1 \end{bmatrix} = C \begin{bmatrix} -A & A^2 & \dots & A^2(1-A)^{n-3} & A^2(1-A)^{n-2} \\ 0 & -A & \dots & A^2(1-A)^{n-4} & A^2(1-A)^{n-3} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \dots & -A & A^2 \\ 0 & 0 & \dots & 0 & -A \end{bmatrix} \begin{bmatrix} V_{Ln} \\ V_{Ln-1} \\ \vdots \\ V_{L2} \\ V_{L1} \end{bmatrix}. \tag{3.29}$$

Using the charge balance relationship, where $Q' + Q = 0$, then an expression for the voltage levels can be derived, where

$$\begin{bmatrix} Q_n + Q'_n \\ Q_{n-1} + Q'_{n-1} \\ \vdots \\ Q_2 + Q'_2 \\ Q_1 + Q'_1 \end{bmatrix} = CM \begin{bmatrix} V_{Ln} \\ V_{Ln-1} \\ \vdots \\ V_{L2} \\ V_{L1} \end{bmatrix} + CV_{DD} \begin{bmatrix} A \\ A(1-A) \\ \vdots \\ A(1-A)^{n-2} \\ A(1-A)^{n-1} \end{bmatrix} \tag{3.30}$$

which can be re-arranged and simplified to yield,

$$\begin{bmatrix} V_{Ln} \\ V_{Ln-1} \\ \vdots \\ V_{L2} \\ V_{L1} \end{bmatrix} = -M^{-1}V_{DD} \begin{bmatrix} A \\ A(1-A) \\ \vdots \\ A(1-A)^{n-2} \\ A(1-A)^{n-1} \end{bmatrix}. \tag{3.31}$$

where M is

$$M = \begin{bmatrix} -2A & A^2 & \dots & A^2(1-A)^{n-3} & A^2(1-A)^{n-2} \\ A^2 & -2A & \dots & A^2(1-A)^{n-4} & A^2(1-A)^{n-3} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ A^2(1-A)^{n-3} & A^2(1-A)^{n-4} & \dots & -2A & A^2 \\ A^2(1-A)^{n-2} & A^2(1-A)^{n-3} & \dots & A^2 & -2A \end{bmatrix}. \tag{3.32}$$

In order to solve these matrices and achieve a final expression, several values of n are selected from two to five, and the final expressions for $V_{L,h}$ are observed

in each of these cases. From these equations the following expression for $V_{L,h}$ can be extrapolated,

$$V_{L,h} = V_{DD}\frac{A(h-1)+1}{A(n-1)+2}, \tag{3.33}$$

which can be used in combination with (3.28) to compute the final voltage at level n where

$$V_n' = \frac{nAV_{DD}}{(n-1)A+2}, \tag{3.34}$$

which can be used to calculate the precharge factor (k),

$$k = \frac{V_{DD}}{V_{DD}-V_n'} = \frac{(n-1)A+2}{2-A}, \tag{3.35}$$

which can be used to calculate the new value of α_B^* or α_T^*.

The equation for V_n' was verified for an n=4 case, using ideal switches and capacitors. A capacitor bank structure was used, for the $n = 4$ case of Figure 3.1, in which the bank capacitors were a factor of 100 times larger than the load capacitor, in order to eliminate any voltage ripple on the capacitors. The testbench was setup to match the assumptions used in the calculations. Next, the on resistance of the switches was varied, with T_{EQ} being held constant. The resulting final value of V_n' was recorded, and is plotted in Figure 3.9, against the calculated. The relative standard error between the calculated and simulation data was 0.4%, indicating the results are quite accurate.

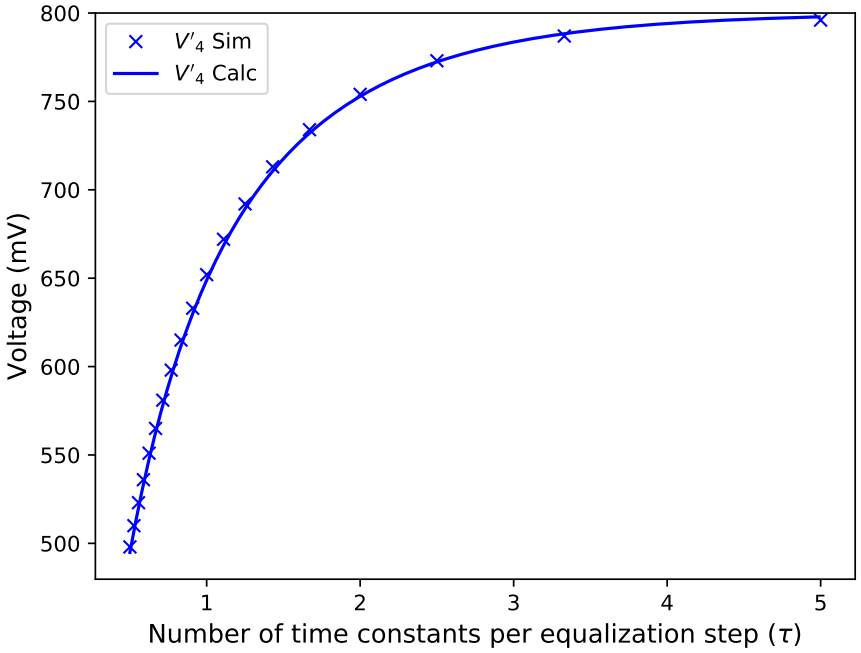


Figure 3.9: Comparison between the calculated V_4' and the simulated for a load capacitor undergoing n=4 charge reuse with a $V_{DD} = 1\,\mathrm{V}$.

Chapter 4

Capacitor Bank Charge Reuse

The results and data described in this chapter were presented at the Midwest Symposium for Circuits and Systems 2019 [24, 26].

4.1 Introduction

Having covered the benefits of charge reuse in chapter 2, there is motivation for a designer to include charge reuse to improve the efficiency of their design. One of the pre-existing methods of implementing this technique is to use time-interleaved cores as in [23]. This technique functions by equalizing the voltage between available cores in the converter.

The issue with this technique is that the intermediary voltage levels must continuously be occupied by a core. This creates a relationship between the level of interleaving and the portion of the period dedicated to charge reuse. Specifically the portion of the period dedicated to charge reuse each cycle is,

$$T_{CH} = T_{SW}\frac{2n}{t_I}, \tag{4.1}$$

where n is the number of charge reuse stages. In the event that the number of time interleaving stages is fixed, potentially a result of minimum capacitor size or control logic overhead, then the designer has limited timing control. One potential solution to this issue is to employ the capacitor bank topology

initially proposed in [25], in which a set of capacitors are employed to store the charge from a capacitive load.

The capacitors forming the bank have finite area however, and thus must be made small relative to the flying capacitors so as to minimize the area cost of this implementation. The resulting trade-off between capacitor bank area overhead and the resulting power savings should then be investigated.

4.2 Capacitor Bank Operation

The operation of SC-PC involves charging and discharging the internal parasitic capacitances each clock cycle. When transitioning from a high voltage on the parasitic capacitance to low, the energy stored on the capacitor is typically wasted by shorting the capacitance to ground. As with the prior charge reuse techniques, the capacitor bank functions by storing this charge and using it on the next transition to reduce power consumption.

The capacitor bank is tested and discussed in the context of use with a voltage doubler, as in Figure 4.1 [6]. An example of an n=2 capacitor bank is present in Figure 4.2, with a corresponding timing diagram in Figure 4.3. A schematic of the proposed capacitor bank is present in Figure 4.4, in which a generic capacitor bank with n levels is illustrated.

Given the limited size of the capacitor bank however, the voltage stored on the capacitors will change depending on the amount of current that flows through them. This will reduce the effectiveness of the charge reuse technique, so the capacitor bank must be sufficiently large to provide adequate performance.

During the equalization with the charge bank, the transistors connecting to both the top and bottom plates are turned off to prevent short circuit currents. The expression for the equivalent parasitic capacitance at the bottom node under these conditions is,

$$C_{par} = C_{Fly}\left(\alpha_B + \frac{\alpha_T}{1+\alpha_T}\right), \tag{4.2}$$

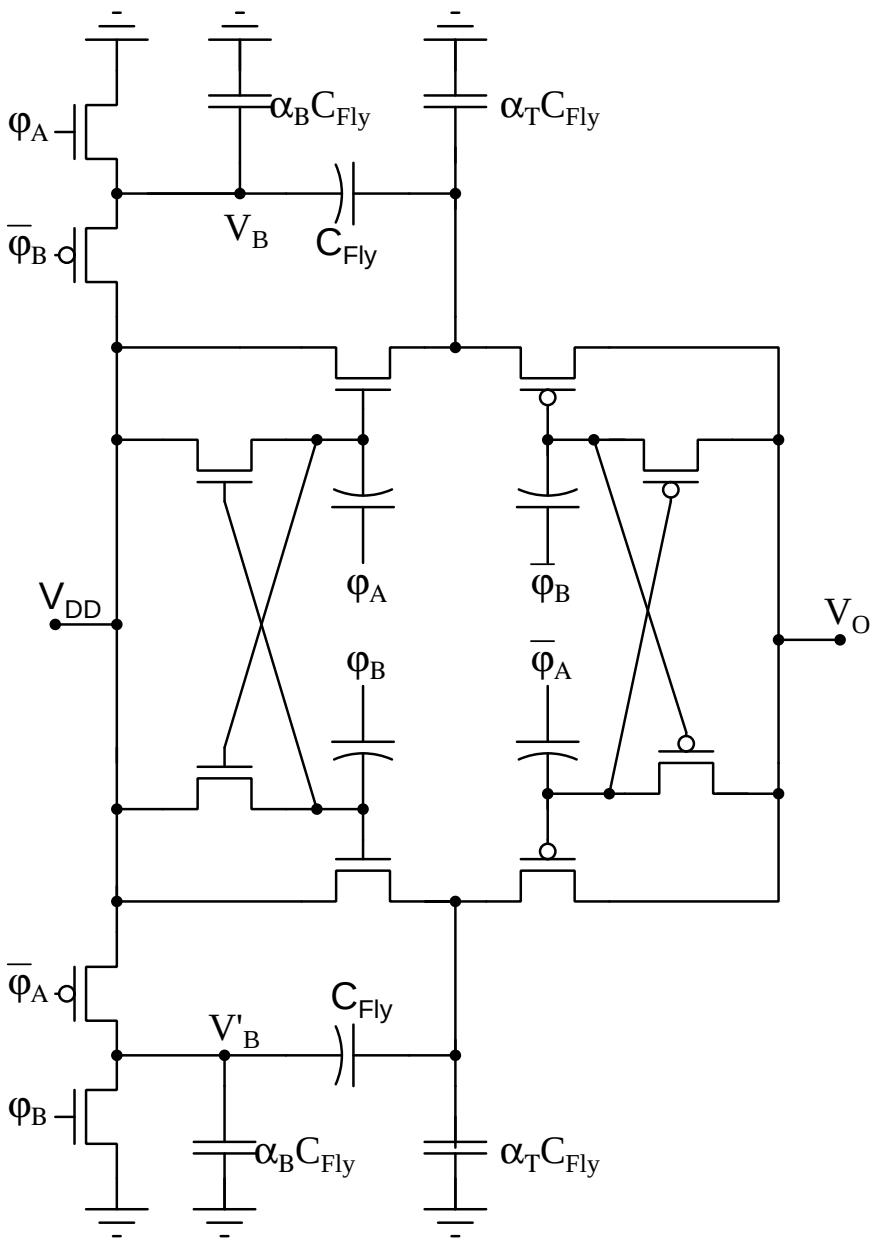


Figure 4.1: Schematic of a voltage doubler with bootstrapping for the pass transistors.

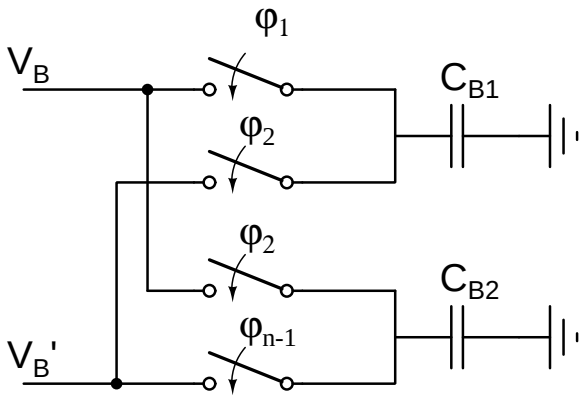


Figure 4.2: Proposed capacitor bank structure for 2 different levels connected to nodes V_B and V_B' of a voltage doubler.

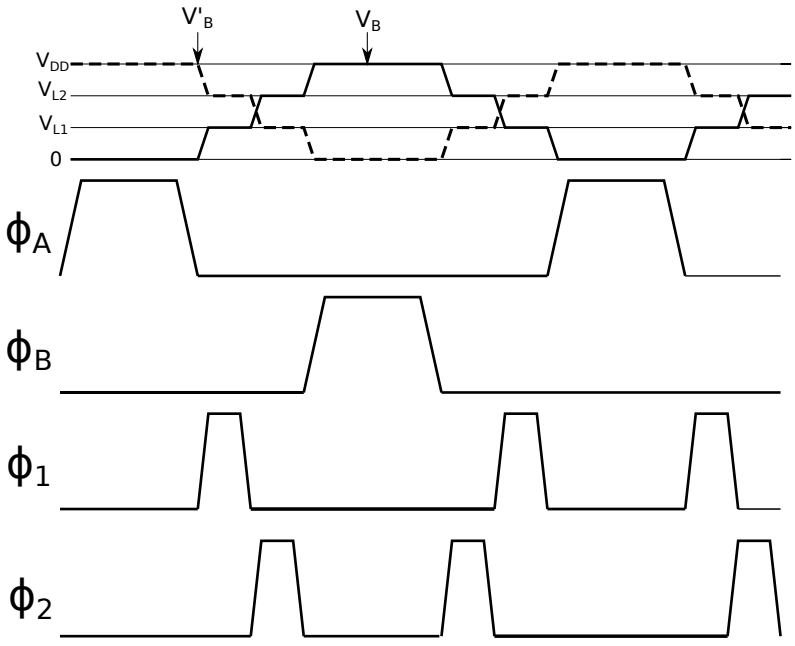


Figure 4.3: Timing diagram corresponding to the n=2 capacitor bank implementation.

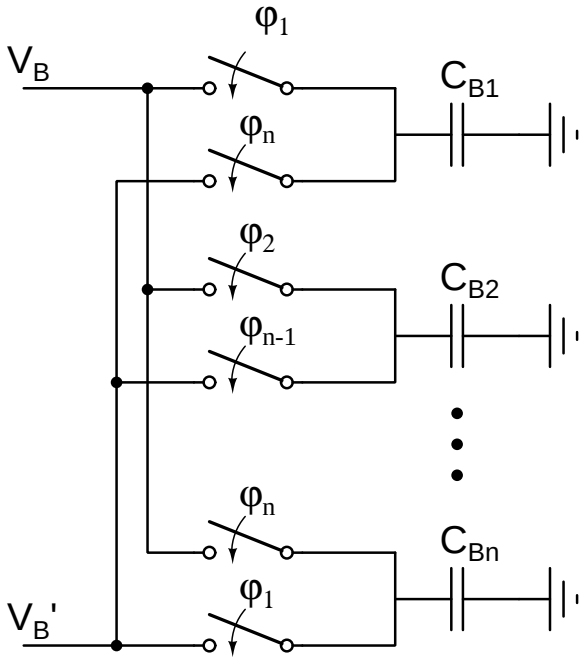


Figure 4.4: Proposed capacitor bank structure for a generic n different levels connected to nodes V_B and V_B' of a voltage doubler.

which can be derived using series parallel reductions for the equivalent circuit at V_B. The series combination of $C_{Fly}\alpha_T$ and C_{Fly} yields an equivalent capacitance of $\frac{C_{Fly}\alpha_T}{1+\alpha_T}$. This parasitic capacitance will then equalize with each of the individual bank capacitors (C_B). The exact expression for the voltage ripple can be acquired by employing a charge balance,

$$C_B(V_{L,h} - V'_{L,h}) + C_{par}(V_{L,h} - V_{par}) = 0, \tag{4.3}$$

where $V'_{L,h}$ is the voltage on the bank capacitor during the previous voltage transition. To explain further, at steady state the voltage on each of the individual bank capacitors will vary between $V_{L,h}$ and $V'_{L,h}$ with $V_{L,h}$ corresponding to the voltage after pulling C_{par} up to V_{DD}. Equation (4.3) can be re-arranged to express the voltage on the bank capacitor in terms of prior voltages,

$$(C_B + C_{par})V_{L,h} = C_B V'_{L,h} + C_{par}V_{par}. \tag{4.4}$$

A set of equations can then be generated describing $V_{L,h}$ as a function of $V'_{L,h}$ where

$$\begin{cases} (C_B + C_{par})\, V_{L,n} = C_B V'_{L,n} + C_{par} V_{L,n-1} \\ \quad \vdots \\ (C_B + C_{par})\, V_{L,2} = C_B V'_{L,2} + C_{par} V_{L,1} \\ (C_B + C_{par})\, V_{L,1} = C_B V'_{L,1} \end{cases} \tag{4.5}$$

which all use the expression for $V_{L,h}$. The equations can be understood by considering the sequence of equalization's that occur, first the parasitic capacitor equalizes with bank capacitor C_{B1}, which has voltage $V'_{L,1}$ stored on it while V_{par} is 0, as the parasitic capacitor is transitioning from the ground state. Next the transistor equalizes with C_{B2}, which has $V'_{L,2}$ stored on it, while the parasitic capacitor has $V_{L,1}$ stored on it from its previous equalization. This continues for all n bank capacitors and generates the prior set of equations. A complimentary set of equations exist describing the voltages on the falling transition,

$$\begin{cases} (C_B + C_{par})\, V'_{L,n} = C_B V_{L,n} + C_{par} V_{DD} \\ \quad \vdots \\ (C_B + C_{par})\, V'_{L,2} = C_B V_{L,2} + C_{par} V'_{L,3} \\ (C_B + C_{par})\, V'_{L,1} = C_B V_{L,1} + C_{par} V'_{L,2} \end{cases} \tag{4.6}$$

which creates enough information to solve for any value of $V_{L,h}$ or $V'_{L,h}$. The solved equations are, The final solution of the equations yields,

$$V_{L,h} = \frac{h C_B V_{DD}}{(n+1)C_B + C_{par}}. \tag{4.7}$$

The expression for $V_{L,n}$ can then be used to calculate the amount of charge required to drive the parasitic capacitor to V_{DD}, where

$$Q^* = (V_{DD} - V_{L,n}) C_{par}. \tag{4.8}$$

This can be compared to the amount of charge typically required to drive a capacitor to V_{DD} from 0,

$$\frac{Q^*}{Q} = \frac{V_{DD} - V_{L,n}}{V_{DD}}. \tag{4.9}$$

Finally, from the perspective of a designer attempting to model the impact of charge reuse on a system, a very useful approximation would be to assume that the parasitic capacitance has been reduced to a new value C^*_{par}. The expanded expression for C^*_{par} is,

$$C^*_{par} \approx C_{par}\frac{Q^*}{Q} = \frac{C_B + C_{par}}{(n+1)C_B + C_{par}}C_{par}. \tag{4.10}$$

4.2.1 Structure Improvements

The first and simplest method of modifying the structure is to remove the center capacitor in odd cases, and instead to equalize the complementary transistors directly. This has the effect of reducing the area overhead of the capacitor bank as a result of the reduced number of capacitors. Additionally, there is a change in the resulting charge reuse effectiveness relative to C_B. The new equation for $V_{L,n}$ is,

$$V_{L,n} = \frac{V_{DD}}{2}\left(1 + \frac{C_B(n-1)}{(n+1)C_B + 2C_{par}}\right), \tag{4.11}$$

which results in an improvement in the effective parasitic capacitance for a given value of C_B/C_{par}.

Another method of improving the capacitor bank structure is to make it differential access using the structure in Figure 4.5. This structure has near identical functionality to Figure 4.4, except that it requires two anti-phase cores in order to function. The associated benefit with the structure is that it requires half of the number of capacitors to operate, and the voltage ripple across each of the capacitors in the bank is shared between the two cores. This has the benefit of reducing the area overhead of the capacitor bank structure by a factor of 4 without decreasing its functionality.

The equation for the voltage levels in the even ordered n is,

$$V_{L,h} = \frac{2hC_BV_{DD}}{2(n+1)C_B + C_{par}}, \tag{4.12}$$

while the equation for the odd ordered dual access is,

$$V_{L,n} = \frac{V_{DD}}{2}\left(1 + \frac{C_B(n-1)}{(n+1)C_B + C_{par}}\right). \tag{4.13}$$

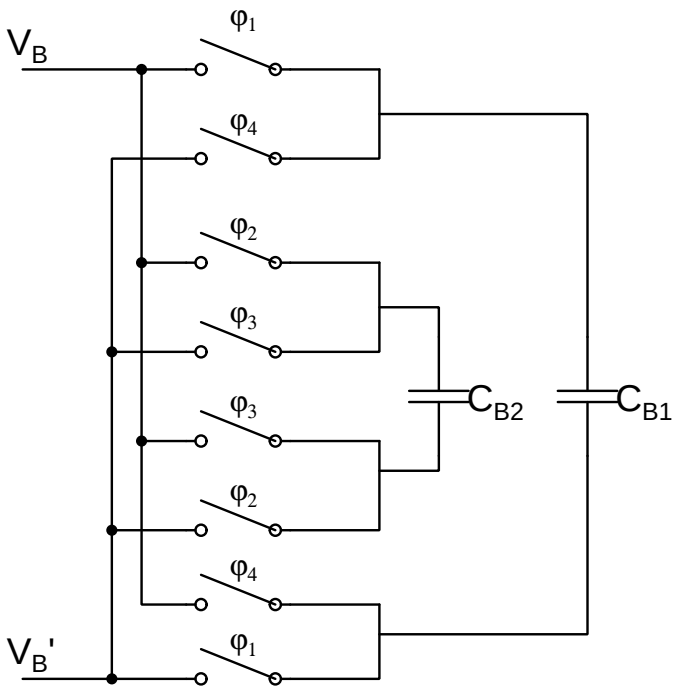


Figure 4.5: Dual access charge pump structure for n=4

4.2.2 Equation Verification

Simulations were run to verify the accuracy of (4.7). The simulated circuit is first run with ideal capacitors and switches. The parasitic capacitor was sized at 30 pF, and a sufficiently long transient was chosen to ensure full equalization. Data is recorded after the circuit has reached steady state conditions. The different voltage levels are plotted in Figure 4.6 for different ratios of $\frac{C_B}{C_{par}}$ for an n=3 case.

Next, simulations were run, substituting the ideal parasitic capacitor for a MOS-capacitor, which has a non-linear capacitance. The motivation here is a result of the fact that the parasitic capacitances associated with the MOS-capacitors are non-linear. The non-linearity results in a discrepancy between the resulting voltage levels and the calculated voltage levels, which can be

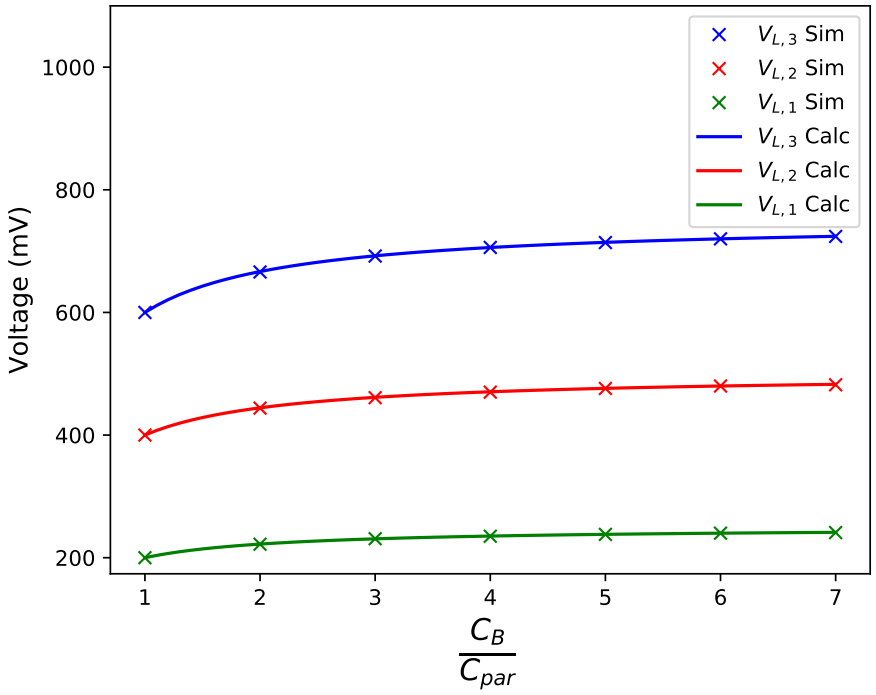


Figure 4.6: Comparison of the calculated voltage levels and those simulated for $V_{DD} = 1$

seen in Figure 4.7. While there is variation from the predicted voltage levels, there are still substantial power savings, and the technique should be viable.

Additionally, the equation describing the charge bank with middle equalization where the capacitor was removed was verified for the $n = 3$ case. The resulting graph of $V_{L,3}$ was plotted in Figure 4.8, where the equation appears to be accurate.

Lastly, the dual access charge bank structure was verified by comparing the value of $\frac{Q^*}{Q}$ to the more standard capacitor bank structure. The comparison can be seen in Figure 4.9, for an n=4 dual access configuration for varying values of $\frac{C_B}{C_{par}}$. The odd ordered test was run for n=3, in which the dual

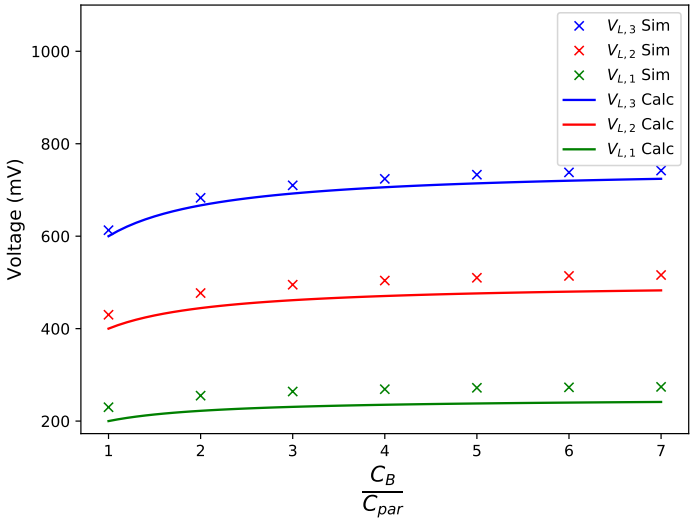


Figure 4.7: Comparison of the calculated voltage levels and those simulated for $V_{DD} = 1$, with a MOS-cap for the load.

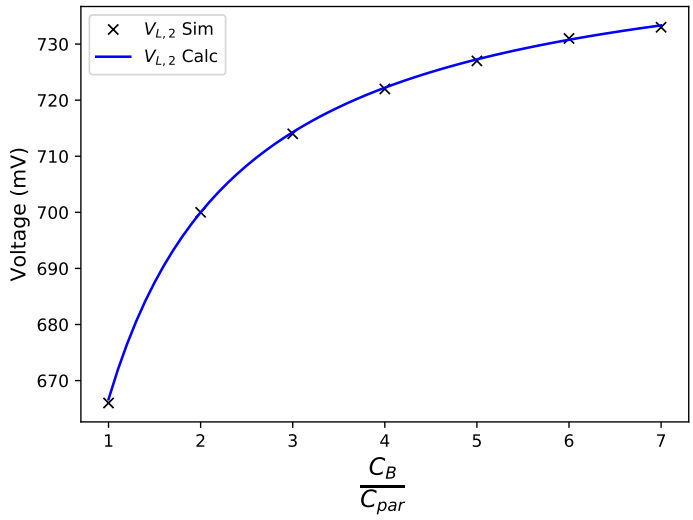


Figure 4.8: Comparison of the calculated voltage levels and those simulated for $V_{DD} = 1$, with direct equalization on the middle level.

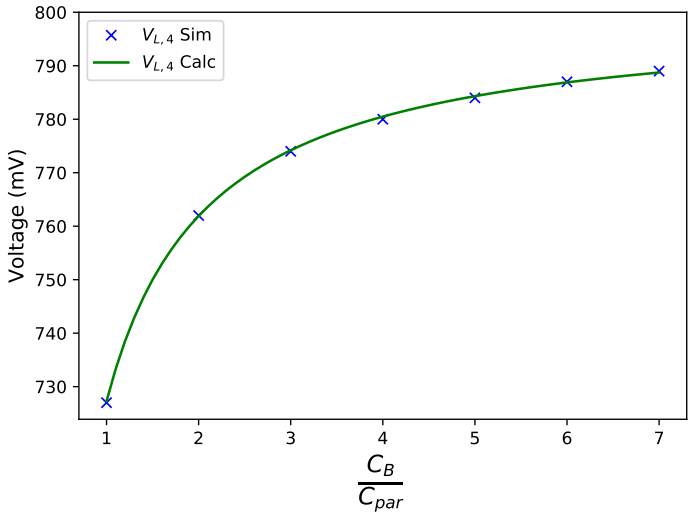


Figure 4.9: Comparison of the calculated voltage levels and those simulated for $V_{DD} = 1$, and n=4.

access capacitor bank was found to outperform the calculated by a substantial margin. This is a result of the direct equalization between on the $V_{L,1}$ level, where a capacitor is not used.

4.3 Design Trade-offs

The area overhead of the capacitor bank can be expressed relative to the size of the flying capacitors,

$$k = \frac{nC_B}{2C_{Fly}}, \tag{4.14}$$

where k is the fractional capacitor area cost dedicated to the capacitor bank. The expression for k can be re-arranged to,

$$C_B = \frac{2kC_{Fly}}{n}, \tag{4.15}$$

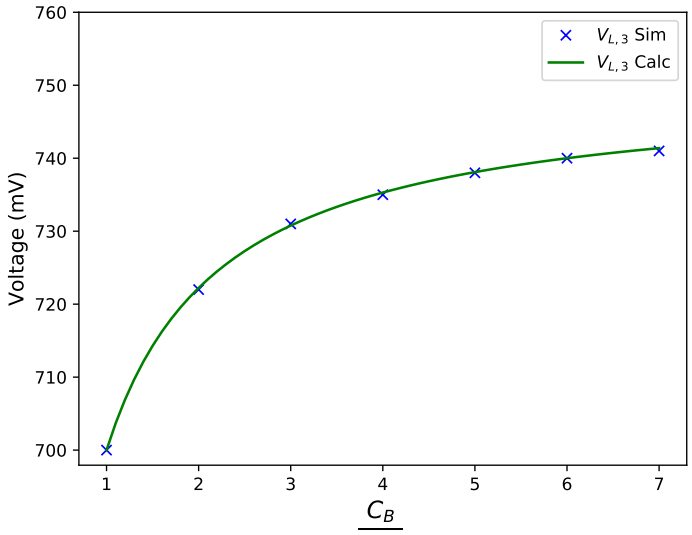


Figure 4.10: Comparison of the calculated voltage levels and those simulated for $V_{DD} = 1$, and n=3 for the dual access capacitor bank.

which can then be substituted into (4.10) in order to relate the area cost of the structure to the reduction of parasitic capacitance

$$\frac{C^*_{par}}{C_{par}} = \frac{2k + \gamma n}{2kn + 2k + \gamma n}. \tag{4.16}$$

It should be noted that the capacitors comprising the capacitor bank do not necessarily need to be the same type as the flying capacitors themselves. The configuration in Figure 4.4 can be implemented using low voltage capacitors, as the voltage stresses can be reduced to $V_{DD}/2$. This reduction in voltage stress is intuitive for capacitors $C_B, 1$ through to $C_{B,n/2}$, which have voltage levels between 0 and $V_{DD}/2$. The solution for capacitors $C_{B,n/2}$ through to $C_{B,n}$ is to wire their bottom plates to V_{DD}, which will reduce their voltage stresses, as their top plates range from $V_{DD}/2$ to V_{DD}. In the case of the TSMC 65 nm library, this would mean that these capacitors could be implemented using the higher density 1 V MOM capacitors, instead of the 2.5 V MOM capacitors, reducing the area overhead of the capacitor bank by a factor of roughly 2.5.

The dual access capacitor bank has an area overhead reduced by a factor of 4 for the even ordered n. The odd numbered banks provide an even larger benefit, as the central equalization level does not require a capacitor.

4.4 Voltage Doubler Simulation

In order to verify the functionality of the capacitor bank in the context of SC power converters, simulations were run using the TSMC 65-nm CMOS technology. The switches were implemented using 65-nm NMOS and PMOS, while the flying capacitors were implemented using 2.5 V devices. The input voltage was set to 1 V, the doubler was designed around an operating frequency of 50 MHz, and the α_B and α_T of the flying capacitors was set to 0.01. Two voltage doubler configurations were tested, one without any charge reuse, and one with n=3 charge reuse implemented using a capacitor bank. The design of the two converters is identical, excluding implementation of the capacitor bank.

A comparison of the different parameters between the two converters can be seen in Table 4.1. The T_{EQ} of the capacitor bank was varied, and the impact of efficiency can be seen in Figure 4.11, in which 1 ns has the best performance across a range of frequencies. A T_{EQ} of 1 ns is used for further simulations.

Next, a set of simulations was run, in which the output voltage of the output is varied, and the operating frequency is held constant at 50 MHz. The power density is measured by recording the output power, and dividing that by the approximate circuit area. The resulting relationship between power density and efficiency is graphed in Figure 4.12, in which the capacitor bank demonstrates higher conversion efficiencies for a range of output powers.

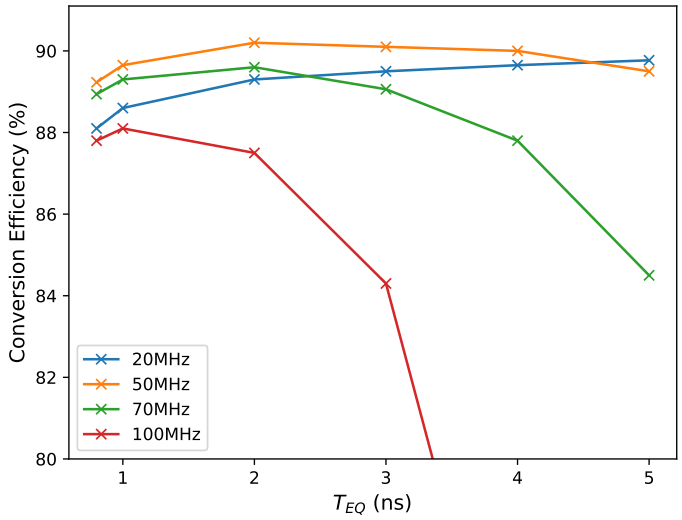


Figure 4.11: Power conversion efficiency versus T_{EQ} for a voltage doubler with an n=3 capacitor bank and V_{OUT}=1.89 V.

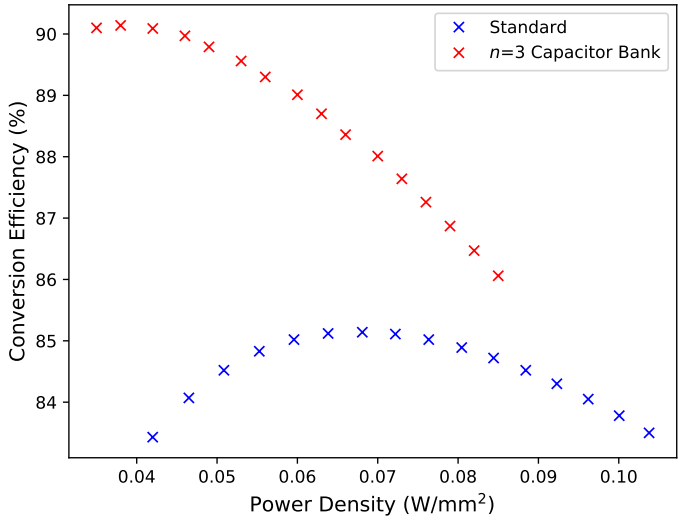


Figure 4.12: Power conversion efficiency versus output power density of the voltage doubler with, and without capacitor bank charge reuse.

Table 4.1: Parameters of Capacitor-Bank and Standard Converters

Parameter	Cap. bank $n = 3$	Standard
C_{Fly} (pF)	200	200
C_B (pF)	10	0
Peak conversion efficiency $\hat{\eta}$	90.1%	85.1%
Area (mm^2)	0.046	0.040
Power density at $\hat{\eta}$ (W/mm^2)	0.04	0.07

Chapter 5

Transistor Control Methods

5.1 Introduction

SCPCs operate by charging and discharging flying capacitors using transistors. In order to fully charge and discharge the capacitor, and achieve high levels of efficiency, the series RC time constant must be considered. The resistance is determined by the channel resistance of the transistor, while the capacitance is the flying capacitance. Thus, the channel resistance of the transistor will dictate how small the time constant is, determining the optimal frequency of the converter. As the frequency of the converter will determine its power density, any techniques which minimize the resistance of the transistors are useful for improving the performance of the converter.

There are a number of circuit level techniques which can greatly improve the performance of SCPCs which result in reduced overdrive voltages of the transistors used [45, 46].

Structures are proposed to improve the performance for different circuit configurations, and the corresponding improvement is analyzed. The structures are investigated in the context of a voltage doubler in the boost configuration. Finally, simulations are run to verify the proposed structures, and the corresponding design trade-offs are analyzed.

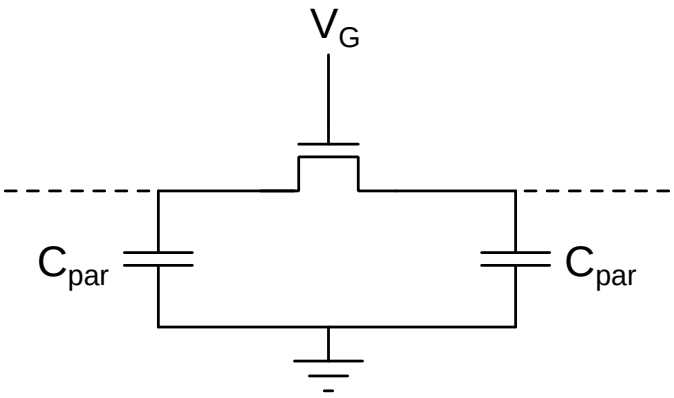


Figure 5.1: Voltage equalization circuit.

5.2 Circuit Technique Analysis

5.2.1 Single Level Voltage Equalization

Voltage equalization techniques are useful for minimizing the amount of power used to charge the parasitic capacitances in a circuit. The simplest voltage equalization technique involves equalizing the voltage on the bottom plate node of the flying capacitor with its complementary node. The equalization transistor initially connects two parasitic capacitors at voltages 0, and V_{DD}, where the gate voltage of the equalization transistor is V_{DD}. However, as the voltages equalize, the source voltage will increase, presumably reaching $V_{DD}/2$.

It can be assumed that the equalization transistor is implemented using an NMOS as a result of its improved carrier mobility. The on resistance of the equalization transistor can be expressed as,

$$R = \frac{L}{Wk'_n(v_{GS} - V_t)}, \tag{5.1}$$

where k'_n is the technology transconductance, W is the channel width, L is the channel length, v_{GS} is the gate to source voltage, and V_t is the threshold voltage. Provided v_G is V_{DD}, then $v_{GS} \approx V_{DD}/2$, as $v_S \approx V_{DD}/2$. If V_t is close to $V_{DD}/2$ this would indicate that $v_{GS} - V_t = 0$, resulting in a very

large increase in resistance. Given the decreasing supply voltage with recent technology nodes, it can be assumed that the overdrive voltage under these conditions will only decrease further.

5.2.2 Multi Level Voltage Equalization

Consider a multi-level voltage equalization system, as proposed in [23], which can be used to reduce the power required to charge the parasitic capacitors by a generic amount. If the number of equalization stages is denoted n, then the power savings are proportional to,

$$P = \frac{V_{DD}^2 C_{par} f_{SW}}{n+1}\,. \tag{5.2}$$

Assuming the parasitic capacitors are linear, then the equalization voltages vary from 0 to V_{DD}, with n intermediary voltage levels spaced between them. From the implementation in [47], the transistors which equalize above $V_{DD}/2$ are PMOS, and the transistors which equalize below $V_{DD}/2$ are NMOS.

The voltage levels each transistor equalizes at are dependent on their position in the equalization chain. For example, the first NMOS to be enabled during the rising transition of a parasitic capacitance will equalize voltages 0 and $2V_{DD}/(n+1)$, resulting in voltage $V_{DD}/(n+1)$. This results in a source voltage of $V_{DD}/(n+1)$, which increase the on resistance, though the increase is less than for the single stage case. Each subsequent NMOS has increased on resistance, as the equalization voltage has increased.

A similar increase in the on resistance is present for the PMOS transistors, which have on resistance,

$$R = \frac{L}{W k_p'(v_{SG} - |V_t|)}, \tag{5.3}$$

The equalization voltages increase from $V_{DD}/2$ to V_{DD}, indicating that the transistors which equalize voltages near V_{DD} have a reduced on resistance in exactly the same way as the NMOS.

In order to deal with the increased on resistance for multi stage equalization, the transistors can be carefully bootstrapped without exceeding the voltage breakdown of the transistors. When the gate voltage of any of the NMOS is high, the minimum voltage at either of its nodes is dependent on the prior equalization state. This means that the NMOS which equalizes at $V_{DD}/2$ could be bootstrapped to achieve near $V_{DD} + V_{DD}/2$ at the gate.

Bootstrapping is likely not a useful technique however, as the minimum gate voltage of the transistors which equalize near $V_{DD}/2$ will be higher. This results in substantial leakage, which will end up increasing the losses in the system, and make the technique less viable.

5.3 Proposed Biasing Method

The proposed biasing method involves regulating the gates of the transistors using a voltage relative to the source voltage of the transistor. This will require an additional capacitor with a bottom plate linked to the node which is the effective source voltage of the transistor being biased.

The exact implementation of the control circuitry will depend on the circuit configuration used. Additionally, the safety of such a technique must be investigated with regard to the voltage tolerances of the transistors used.

5.3.1 Single Stage Voltage Equalization

Consider the case of single stage voltage equalization between two flying capacitors. Assuming the equalization transistor is an NMOS in order to make use of the improved carrier mobility, then the source voltage of the transistor is going to be whichever of the two capacitors is being driven high.

This means that two dynamic bias voltages must be generated, one relative to each flying capacitor. The transistor has 4 states, which are summarized in Table 5.1. Next, the voltage stresses of the transistors connected to each of these nodes must be understood, in order to assess whether breakdown will occur.

Table 5.1: List of possible circuit and node states

State #	A (V)	A' (V)	V_G (V)
1	1	0	0
2	1	0	1
3	0	1	0
4	0	1	1

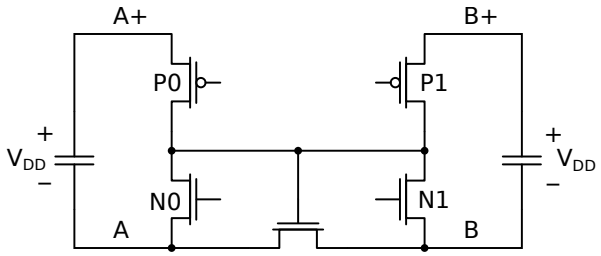


Figure 5.2: Proposed dynamic bias circuit without control voltages

The voltage stress of P1 is highest under state 1, where the drain to source voltage is 2 V, transistor P2 undergoes a similar level of voltage stress in state 3. Transistors N1 and N2 only ever undergo 1 V of stress.

However, the control of the gates of N1 and N2 is difficult, as they have a variable source voltage, where the source voltage of the transistor can be determined by either A, A' or V_G. For instance, in state 1, the source voltage of N1 is 0 as a result of V_G, rather than A. This means that N1 needs to swing between 0 and $V_{DD} + A$, which would mean that a transistor with a thicker oxide is the simplest way to deal with the gate to source stresses. An identical scenario applies to N2.

Transistors P1 and P2 also face similar difficulties with regards to control, their source voltage varies from 2 to 1 V, indicating that gate voltage swings of 1 V will be insufficient to completely turn them on and off. Given the increased voltage stress the transistors are under, thick oxide transistors with wider gate voltage swings will result in the simplest method of control.

5.3.2 Multi Stage Voltage Equalization

The multi stage voltage equalization can use an identical bias circuit to Figure 5.1, and all the transistors that make up the equalization can be created using NMOS transistors, reducing their on resistance.

5.3.3 Dynamic Bias Voltage Generation

The next detail of interest to designers is the method by which the voltage stored on A_+ is generated, as well as the sizing of the bias capacitors.

The sizing of the bias capacitors must be several times that of the gate capacitance they drive, a conservative estimate would likely be a factor of 20. The voltage swing on the bias capacitor can be calculated,

$$\Delta V_{Bias} = \frac{V_{DD} C_G}{C_{Bias}}, \tag{5.4}$$

where C_G is the sum of the individual gate capacitances of all the unique transistors driven by C_G. Lastly, there is an additional component contributing the the change in V_{Bias} resulting from the top plate parasitic capacitance. The final expression for ΔV_{Bias} is then,

$$\Delta V_{Bias} = \frac{V_{DD} C_G}{C_{Bias}} + \beta V_{DD}. \tag{5.5}$$

As such, β should ideally be small to ensure that the produced bias voltage remains as high as possible.

The bias generation is highly dependent on the circuit technique being used, potentially allowing for the re-use of existing structures in the converter.

5.4 Bias Generation

The bias generation is simplest in the case when the existing flying capacitors can be used, and the voltage A is at known states within the converter.

5.4.1 Flying Capacitor Re-Use

One of the simplest methods of implementing the bias capacitors is to use the existing flying capacitors in the converter. Consider the case of a voltage doubler in the boost topology where the bottom plate equalization is used. The first stage of the doubler is going to have V_{DD} stored across it, making it ideal for use in the biasing of the transistors, especially as the bottom plate of the capacitor is already connected to the source of the transistors. The flying capacitor is going to be many times larger than the gate capacitance of the equalization transistors, as their gate capacitance is going to be a small fraction of α.

This method of flying capacitor re-use should be useful for single, and multi-stage voltage equalization, as the common source voltage with the flying capacitors in the converter can be exploited. In the case of multiphase soft charging however, this technique is not as readily available, given that the voltages to be generated can be substantially higher than V_{DD}. Additionally, in the case of the continuous conversion ratio circuit, the flying capacitors only have V_{DD} stored on them for a fraction of the period, though the existing structure proposed has the bias voltages generated externally already.

5.4.2 Multiphase Bias Generation

The primary issue associated with generating the bias for the multiphase soft charging structure is that the voltage stored on the flying capacitors can drop substantially far below V_{DD}. When the voltage drop across the flying capacitor is large is exactly the scenario when the transistors making the intermediary connections need to be biased. There does not exist a voltage in the converter relative to any of the intermediary voltages V_{I1}, V_{I2} indicating that one must be created, which will require additional area.

In the doubler configuration, the bias generation can be achieved using a configuration similar to that of a Cockroft-Walton. An example of the bias generation circuit can be seen in Figure 5.3, where the bias voltage is generated

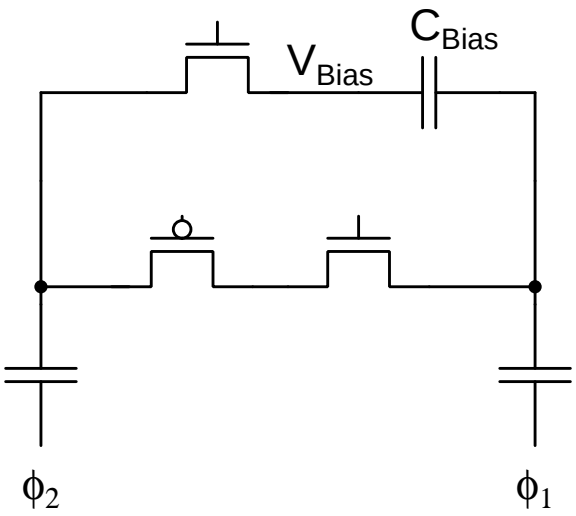


Figure 5.3: Bias generation for top plate relative voltages in a voltage doubler, control of the connection transistors not labeled

between stages in the converter spaced apart by V_{DD}. Assuming a ratio of 20:1 between C_{Bias} and C_G, then the capacitance overhead of the bias network is roughly 20 times that of the interconnection transistors.

5.4.3 Transistor Control

In order to regulate the currents through the transistors in Figure 5.1, the NMOS and PMOS transistors require gate voltages between 0 and $2V_{DD}$ to prevent short circuits. This requires the use of level shifters to translate logic levels of 0 to V_{DD}, while using minimal area and circuit overhead.

There exist a substantial number of level shifters in the literature which occupy minimal area and use relatively minimal power. However, given the conditions in which these level shifters will be used, a level shifter can be designed for the specific application.

A simple level shifter that uses the minimal amount of power per transition is the bootstrapped level shifter in Figure 5.4. The only transistors making

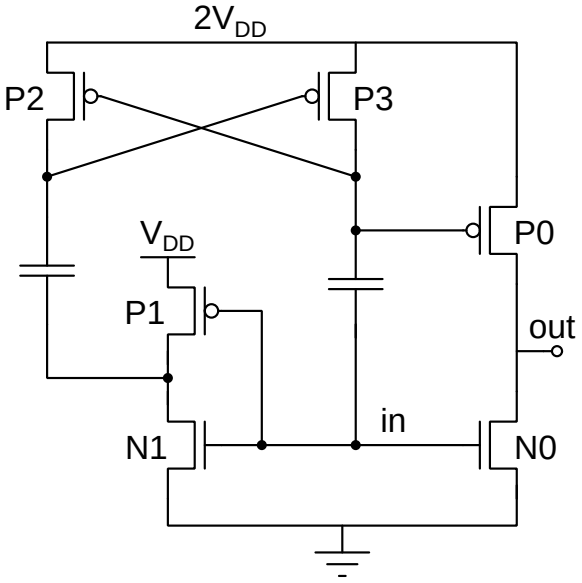


Figure 5.4: Low power, high speed level shifter

up the level shifter which are high voltage are N0 and P0, while the rest of the transistors are made up of the smaller, lower power transistors.

5.4.4 Low Voltage Transistor Implementation

An alternate gate control structure which uses exclusively low power transistors, is the one in Figure 5.5. The structure is somewhat complicated, resulting from the different ranges of voltages available at the gates, and the voltage tolerances of the structure.

The different states of the structure are as follows,

5.4.4.1 A : A_+

This transition uses the PMOS transistor chain, and occurs when A=0, and B=V_{DD}. The gate of P0 switches from A_+ to A, and current conducts, driving the gate up to A_+. N1 stays within acceptable voltage ranges, as its gate and source voltages are A. N3 has gate and source voltages of B, which stays within

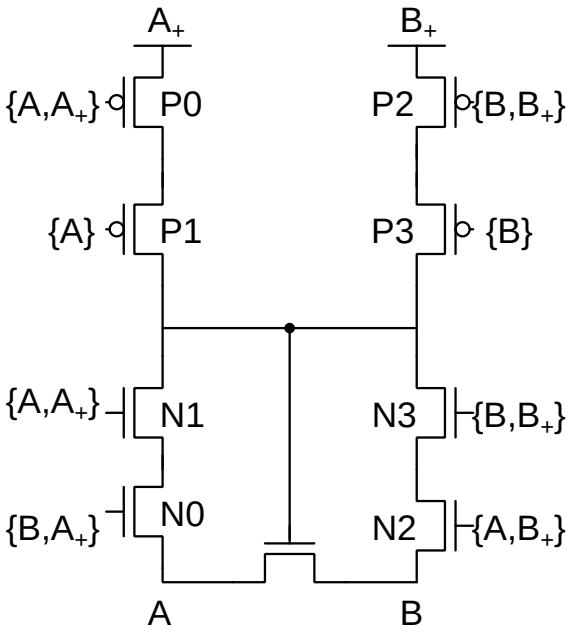


Figure 5.5: Low power implementation of the equalization control circuitry, the voltages at the gates are labelled. The conduction state is listed on the right, while the current blocking state is listed on the left.

breakdown, as B is a higher voltage than A during this state. Lastly, P3 stays within acceptable ranges, as the gate voltage is B, and functions to shield P2 from the large voltage drop.

5.4.4.2 A_+ : B

This transition occurs immediately after the voltages at the two nodes equalize, before B drops to 0 and A increases to V_{DD}. N3 and N2 can conduct current, as $V_{GS} = B_+ - B = V_{DD}$, N0 functions to block current through A with its gate voltage of B, and both P0 and P2 have gate voltages equal to their source, disabling them.

None of the transistors exceed their breakdown, while A_+ is $2V_{DD}$ higher than B, P1 shields it from the low output voltage.

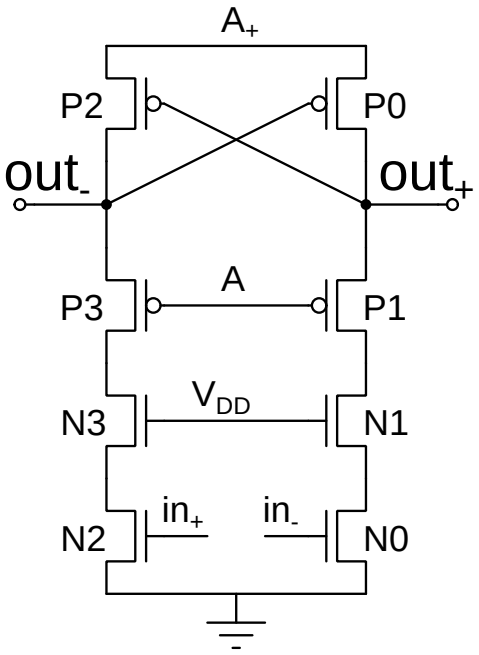


Figure 5.6: Level shifter comprised of low voltage transistors

5.4.5 Variable Supply Level Shifter

The transistors in Figure 5.5 require gate control which cannot be boot-strapped, as the voltages of A and B vary relative to the supply logic levels. As a result, a level shifter which operates without decoupling capacitors must be designed. The typical low voltage level shifter should work relatively well, which can be seen in Figure 5.6. The output of the level shifter transitions between A_+ and A, which can then be used to drive an inverter, an equivalent circuit can be used to generate voltages between B and B_+.

The transistors are sized according to Table 5.2, where the majority of the transistors are sized minimally, excluding P1 and P3. P1 and P3 must be sized larger to ensure they can pull the output down to A quickly and properly generate a logic 0.

Table 5.2: Transistor sizing corresponding to Figure 5.6

Transistor	Width (nm)	Length (nm)
N0-N3	120	60
P0	120	60
P1	360	60
P2	120	60
P3	360	60

5.5 Circuit Simulation

In order to verify the effectiveness of the proposed circuits, they are simulated using the TSMC 65 nm technology library. The testbench used for verifying the dynamic bias can be seen in Figure 5.7, which allows for the control of the equalization voltage.

The M0 transistor is implemented exclusively using an NMOS in the case of testing the dynamic bias control. For the comparison cases with traditional digital control, M0 must be tested both as a PMOS and NMOS for different values of V_{EQ}. The dimensions on M0 are held constant at a W/L of 16.6, using a channel length of 60 nm, the supply voltage is held constant at 1 V. Lastly, V_{OUT} is held at 2 V, and $C_{par} = 0.02C_{fly}$, where C_{fly} is 70 pF.

The results are recorded in Figure 5.7 which indicate a substantial improvement in on resistance for almost all equalization voltages in the NMOS case. For the PMOS, as a result of the reduced carrier mobility, a substantial improvement in equalization time is observed, particularly near $V_{EQ} = 0.5$ V.

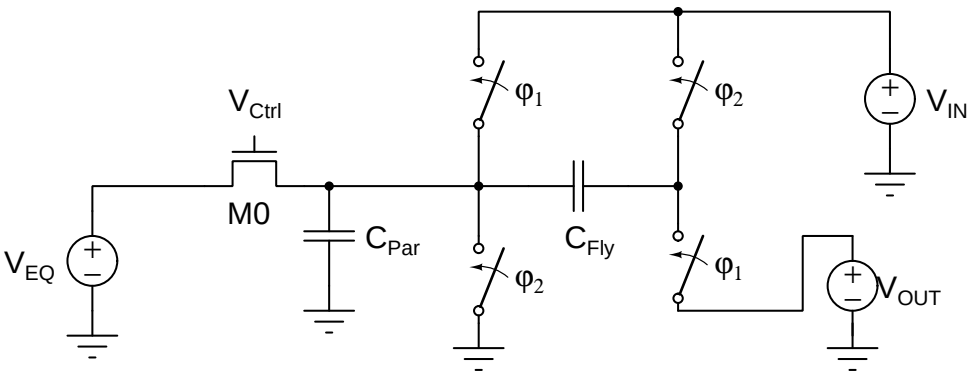


Figure 5.7: Dynamic bias testbench setup, V_{Ctrl} is implemented using either the proposed dynamic bias circuit, or digital logic.

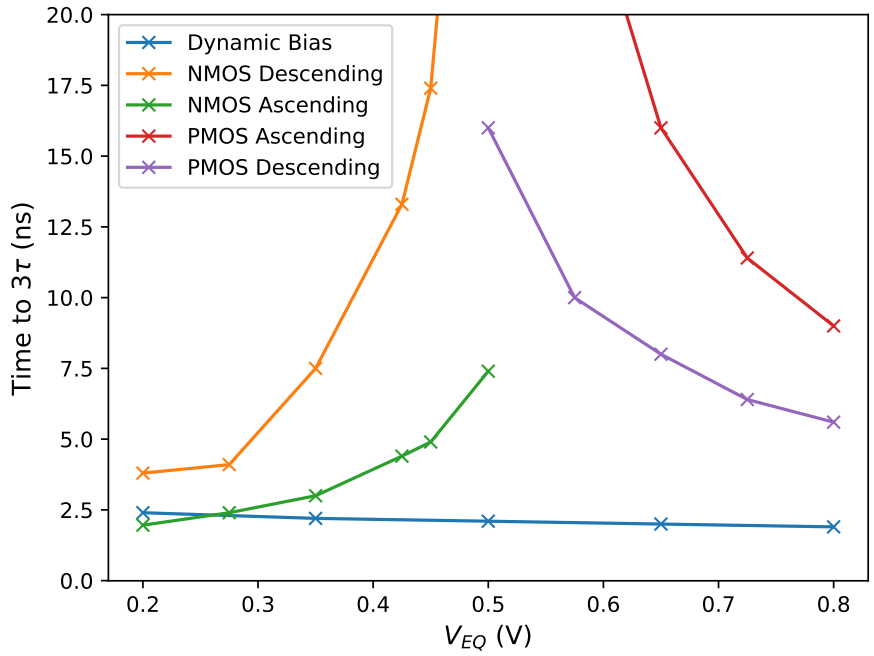


Figure 5.8: Time required to equalize the parasitic capacitor to 3τ voltage drop, including both the pull down equalization time and the pull up.

Chapter 6

Conclusion

6.1 Discussion

The presented analysis of generic n stage charge reuse indicates a method of transforming existing SCPC models to accommodate the resulting changes. As the analysis is performed on the core SC cell, and not on the SC structure as a whole, the results should accurately reflect the impact on networks of SCPCs. Additionally, the presented models for incomplete charge transfer appear to be accurate based on the simulation results, indicating they are appropriate for use in the design process.

The proposed capacitor bank structure can be used to easily implement n stage charge reuse. The area overhead of the structure is calculated, and the resulting structure is simulated for use in combination with a voltage doubler designed using TSMC 65 nm fabrication technology. The resulting peak efficiency of the simulated $n = 3$ capacitor bank was simulated at 90.1%, while the corresponding equivalent circuit without charge reuse had an efficiency of 85.1%. The area overhead of the capacitor bank was 15% of the flying capacitance area for the given implementation.

The impact of odd ordered capacitor bank implementations was also simulated and calculated. The result reduced the number of capacitors by 1, while

resulting in a rough doubling of the resulting effective C_B size. The proposed dual access capacitor bank was found to decrease the required area for the implementation by a factor of 4. This would reduce the area overhead of the prior capacitor bank implementation from 15% to roughly 1%. Assuming the designer is limited to 5-6 levels of charge reuse as a result of the timing consequences, then the area overhead of the capacitor bank in the dual access implementation will be proportional to $\alpha_T + \alpha_B$. This is a small cost, relative to the resulting improvements in efficiency.

The dynamic biasing method proposed reduces the time required for charge reuse equalization as shown by the simulations. This will make the charge reuse techniques substantially more viable by reducing the timing consequences of equalization.

6.2 Future Work

There are a number of ways in which the presented work could be expanded or built upon. One of the most obvious ways would be to fabricate a chip which compares the techniques to a typical SCPC which does not use them in order to further verify the equations and models used. Additionally, combinations of some of the techniques from the literature could be covered.

One highly promising technique in the literature not heavily investigated in the work is the multiphase soft-charging technique proposed in [18]. The technique should result in substantial efficiency improvements in multi-stage power converters, and should interact well with charge reuse techniques. The benefits associated with combining the two techniques could result in benefits when compared to either of the techniques in isolation.

An additional topic not heavily discussed is the impact of charge reuse on multi stage SCPC. Lastly, additional work could be done to verify the impact of dynamic biasing on the performance of SCPCs more directly, in which the technique is specifically simulated in combination with a SCPC. This would

add further validity to the technique, and highlight any issues associated with the design.

Published Papers

- **M. Lipski** and S. Gregori, "Switched-capacitor power converters with soft charging via auxiliary capacitor bank," in *2019 IEEE Int. Midwest Symposium on Circuits and Systems (MWSCAS),*, Aug. 2019, pp. 810–813.
- **M. Lipski** and S. Gregori, "Analysis of charge reuse in switched-capacitor power-converter drivers," in *2019 IEEE Int. Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 2019, pp. 742–745.
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